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2-GHz, 12-bit PCI Express digitiser

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Cognitive radio arrives, all by itself!

BY PATRICK MANNION, BRAND DIRECTOR, EDN

A scant 10 years ago, it seemed that the ultimate in cognitive-radio concepts was considered to be so far out there that it would always be a pipe dream without massive government expenditure on research and infrastructure. So how did it just "happen"? It was Joseph Mitola III who coined the term cognitive radio and defined it as radio that is "self-aware, user-aware, [and] RF-aware" and that incorporates elements of "language technology and machine vision." Back in 2004, in conversations I had with Mitola, then working at Mitre, and Bruce Fette, then with General Dynamics, it seemed the foundations of cognitive radio were just beginning to be put into place.

Software-defined radios that could adapt to multiple wireless baseband processing and modulation/demodulation schemes were a hot topic, fed in part by the emergence of new multicore processing architectures with less and less power consumption. At the front end, higher levels of CMOS integration offered by the emergence of direct-conversion radios and other techniques made flexible front ends seem likely to match the flexible processing architectures. Even the Federal Communications Commission was cooperating, opening up more spectrum and looking for ideas on how to mitigate in-band interference with the licensed radios operating regionally.

Everything seemed to be coming together, but there were some really important issues that needed to be addressed to fully realize the potential of a handset that, in Fette's words, could not just avoid being an interferer and adapt to multiple bands but also be cognizant enough to remind you when you were approaching a pothole you hit last time you went a certain route in your car.

In 2004, the intelligence, processing power, and contextual location-awareness requirements for the latter were just not feasible. So it remained a pipe dream. For the former, there was talk of using RF MEMS as the foundation for programmable bandpass filters that could tune to any band, without the need for multiple RF front ends. The signal would go from antenna, to filter, to digital. But RF MEMS were still too nascent.

At that time, I also spoke with a fellow by the name of Gerald Q Maguire, a professor at the KTH Royal Institute of Technology (Stockholm, Sweden), who made a very important connection between advances in wireless and ever-cheaper memory. In fact, he considered it critical. I agreed. But store that thought for a second.

Fast-forward to 2013, and look at what has happened. Starting with the iPhone and its multisensory, multi-band, location-aware capabilities with increasing amounts of memory coupled with an ecosystem of software (app) developers, and suddenly you have what no government, no single group, and no organization could have conceived or enabled: fully-aware handsets that can adapt to multiple bands and tell you everything about where you are and where you've been. (Ask the NSA.) And voilà! Cognitive radio has arrived. All by itself. That part about flexible RF front ends is still a bit of an issue, but earl;y last month (June 4) I was encouraged by the announcement by Cavendish Kinetics that it was sampling tunable RF capacitors based on the company's "patented breakthrough RF MEMS technology." I hope it works, but either way I was inspired enough to reflect upon how far we've come in 10 years.

I look at my kids sometimes and I literally can't imagine what's next, what world they'll live in. Can you?

Contact me at patrick.mannion@ubm.com.

A valediction...

On page 11 of this issue you'll find column by Howard Johnson, signing-off from his Signal Integrity column after many years of contributions to EDN. His regular insights have been invaluable to many readers, and I hope you'll join me in offering Howard our best wishes for whatever he turns his attention to in the future.

Graham Prophet

pulse

MEMS resonator and oscillator circuitry integrated onto single IC

Silicon Labs, using MEMS technology it acquired when it bought Silicon Clocks, has introduced a wide-frequency-range oscillator that uses a MEMS resonator fabricated on the same die as the oscillator and frequency synthesiser. Silicon Labs says it has used the two years since that acquisition in developing the integrated MEMS technology to enable production of high-volume, low-cost oscillators on a standard CMOS foundry process.

The company's Si50x CMEMS oscillators represent a "leap ahead of quartz-based timing devices with superior frequency stability, reliability and programmability" Silabs asserts. It has designed them to replace general-purpose crystal oscillators (XOs) in cost-sensitive, low-power and high-volume industrial, embedded and consumer electronics applications. CMEMS technology enables MEMS structures to be built directly on top of standard CMOS wafers; the process first fabricates the oscillator and frequency synthesiser circuitry, then planarises the wafer, deposits silicon on top, and fabricates the MEMS section in that silicon.

A single MEMS resonator reference frequency is used – 25 MHz – and the mode of resonance is in the plane of the silicon die – in this device, MEMS flexing is in the X/Y directions only, parallel to the wafer surface, not along the Z axis. Temperature stability is enhanced by combining silicon and SiO2 patterns in the MEMS element; these material have opposing responses to changes in temperature and increase the inherent stability of the MEMS resonator's frequency by passive compensation. Active temperature temperature compensation is also used and is enhanced by the fact that the resonator, sensor and compensation circuitry are closely coupled on the same die. This results in a frequency/temperature characteristic that is almost flat through the standard industrial operating temperature ranges, and when exposed to temperature transients, and

that shows none of the cubic response typical of a crystal.

The oscillator family achieves smaller size, higher reliability, better aging and higher integration than existing frequency control solutions; Silabs adds that CMEMS technology enables guaranteed data sheet performance with 10 years of frequency stability; the specified figure includes ageing, solder shift, load pulling, VDD variation, operating temperature range, vibration and shock. This guaranteed operating life performance is 10 times longer than typically offered by comparable crystal and MEMS oscilla-

The MEMS resonator is fabricated in the top layers of the CMEMS process.

tors.

The Si50x CMEMS oscillators support any frequency between 32 kHz and 100 MHz. Frequency stability options include ±20, ±30 and ±50 ppm across extended commercial (-20 to 70C) and industrial (-40 to 85C) operating temperature ranges. Ageing, com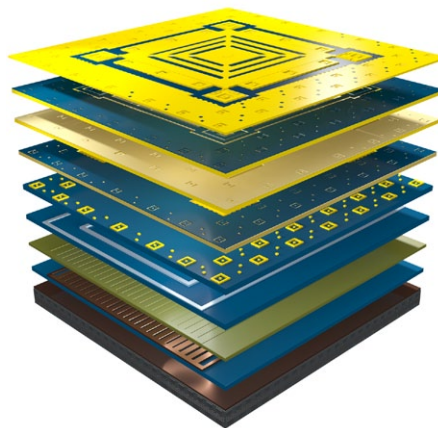pared to typical competing crystal products, is almost negligible, Silabs says. The CMEMS oscillators also offer extensive field- and factory-programmable features including low-power and low-period jitter modes, programmable rise/fall times and polarity-configurable output-enable functionality.

With the Si50x CMEMS oscillator family,

you do not have supply chain problems that are typical for traditional quartz-based solutions, Silabs adds; because CMEMS oscillators are integrated, monolithic ICs, they are packaged in widely produced, moulded-compound 4-pin packages, again ensuring a predictable and reliable supply chain.

The Si50x oscillators are available for web-based customisation with two-week sample lead times or optionally available with "0-day" lead time via instantaneous field programming at the customer's site by Silicon Labs' sales channel partners. The oscillators are pin- and footprint-compatible with existing quartz or MEMS oscillators, enabling a quick, easy drop-in replacement solution. The Si50x family comprises four products with many possible configurations. Si501 is a single-frequency oscillator with output-enable (OE) functionality; Si502 is a dual-frequency oscillator (two programmed, selectable output frequencies) with OE and frequency-select (FS) functions; Si503 is a quad-frequency oscillator with FS; and Si504 is fully programmable oscillator supporting all potential configuration features with a 1-pin interface for fine-tuned frequency adjustments measured in parts per billion – in this variant, the output frequency programming is not stored in non-volatile memory, but must be loaded at power-up.

Other features include the ability to set drive strength (output power); there is a capability to trade-off output jitter against power consumed by the devices, from lowest current of 1.7 mA to lowest jitter of 1.1 psec RMS. Output edge rate can be controlled to minimise EMI issues. Silabs says that the technology is extensible to high-stability performance levels and expects it to compete with more expensive crystal oscillator types in future developments.

The CMEMS oscillators come in three industry-standard 4-pin DFN package sizes: 2 x 2.5 mm, 2.5 x 3.2 mm and 3.2 x 5 mm. Pricing begins at $0.44 (10,000). The Si501-2-3-4-EVB Evaluation Kit is priced at $99 and hosts a pre-programmed Si504 device and open sockets in each package size. More at; www.silabs.com/CMEMS

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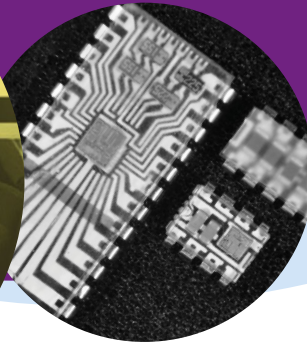
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Silabs acquires Energy Micro

In a separate recent announcement, Silicon Labs signed an agreement to acquire Energy Micro AS, based in Oslo. Energy Micro sells what it describes as the industry's most power-efficient portfolio of 32-bit "energy-friendly" microcontrollers and is developing multi-protocol wireless RF solutions based on ARM Cortex-M architecture. Silicon Labs says that this deal positions the company as the foremost innovator in energy-friendly embedded solutions. Energy Micro's portfolio contains 32-bit Precision32 MCU, Ember ZigBee and sub-GHz wireless products for the embedded market. The acquisition expands Silicon Labs' MCU portfolio, adding nearly 250 ARM-based EFM32 Gecko MCU products ranging from extreme-low-power, small-footprint MCUs based on the ARM Cortex-M0+ core to higher-performance, energy-friendly MCUs powered by the Cortex-M4 core capable of DSP and floating-point operations. The companies' statement also says that the acquisition is expected to enhance Silicon Labs' radio portfolio with the addition of Energy Micro's ultra-low-power EFR Draco radio products. These wireless transceivers and system-on-chip (SoC) devices will support frequency bands ranging from sub-GHz to 2.4 GHz and multiple standard and proprietary protocols including Bluetooth Low Energy (LE), 6LoWPAN, ZigBee, RF4CE, 802.15.4(g), KNX, ANT+ and additional protocols.

Silicon Labs says it intends to apply these complementary embedded technology platforms and expertise to the IoT (Internet of Things) and smart energy markets, as well as battery-powered portable electronics devices. Both companies' 32-bit MCU and wireless products use the same ARM Cortex-M architecture.

Silicon Labs, www.silabs.com
Energy Micro, www.energymicro.com

Tek will use IBM 9HP SiGe technology to take scopes to 70GHz

Tektronix has confirmed that its next generation of high performance real-time oscilloscopes will incorporate IBM's latest 9HP silicon-germanium (SiGe) chip-making process. This fifth generation of IBM's semiconductor technology along with other advances such as the Asynchronous Time Interleaving that Tek announced previously will result in oscilloscopes with bandwidth capability of 70 GHz and improvements in signal fidelity. Operating at speeds (fT) up to 350 GHz, 9HP is the first SiGe technology featuring the density of 90nm BiCMOS and delivers higher performance, lower power and higher levels of integration than current 180nm or 130nm SiGe offerings. Tek previously previewed its next series of high-performance oscilloscopes, promising a 2014 release for units with real-time bandwidth of 70 GHz, for applications such as 400 Gbps and 1 Tbps optical communications and fourth generation serial data communications.

"By extending our long-standing relationship with technology leader IBM, Tektronix is continuing to push the envelope on what can be achieved in high-fidelity, high-speed data acquisition systems. Early adoption of 9HP has allowed our engineers to explore innovative architectures and performance thresholds once thought unattainable," said Kevin Ilcisin, chief technology officer, Tektronix. "The advanced 9HP SiGe BiCMOS technology provides the faster switching speeds, high integration levels, and low noise our next generation of performance instrumentation requires to meet customer requirements." Tektronix' forthcoming oscilloscopes will use Asynchronous Time Interleaving technology to improve signal-to-noise ratio beyond the standard frequency interleaving approach in use today. In traditional frequency interleaving, each analogue-to-digital converter (ADC) in the signal acquisition system only sees part of the input spectrum. With Asynchronous Time Interleaving, all ADCs see the full spectrum with full signal path symmetry. This offers the performance gains available from interleaved architectures but without the same impact to signal fidelity. There's more in a paper for download, "Techniques for Extending Real-Time Oscilloscope Bandwidth."

Test for USB 3.0

Tek has also announced a test solution for 10 Gbps SuperSpeed USB. A series of enhancements to its USB 3.0 test solutions includes a transmitter test solution for the SuperSpeedPlus 10 Gbit/sec specification. Other enhancements include a new USB 3.0 oscilloscope-based layered decode capability and an enhanced automated solution for SuperSpeed USB transmitter testing that improves test throughput by up to 60%.

With the faster data rates for USB 3.0 come new test challenges, most notably major increases in channel loss and reduction in signal to noise ratio as well as more complex link training and timing requirements that must be verified. Tektronix' USB 3.0 decode software has protocol-specific triggering, search and navigation, and multi-layer decode. This allows the user to easily navigate through the protocol stack, fully time correlated with the analogue waveform on the same screen.

The new TekExpress USB 3.0 transmitter test software (Option USB-TX) and SuperSpeedPlus USB transmitter test software (Option SSP) will both be available for download on www.tek.com in July 2013.

The principle of Asynchronous Time Interleaving that will enable scope bandwidth of 70 GHz.

The USB 3.0 decode will be a free upgrade for customers with a DPO/DSA/MSO70000 Series Oscilloscope with option SR-USB which will be available in July 2013.

Tektronix; www.tek.com

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Elliptical curve asymmetric key authentication solutions from Atmel

Expanding its CryptoAuthentication Portfolio, Atmel's lower-cost ATECC108 product offers lower bill of material by delivering an easy-to-use one-chip security solution that is suitable for consumer, medical, industrial and automation applications. It embodies security features that support some of the latest security standards from the National Institute of Standards and Technology (NIST) including the P256, B283 and K283 elliptical curves, and FIPS 186-3 elliptical curve digital signature algorithm. With up to 8.5 kb EEPROM, allowing storage for up to 16 keys, a unique 72-bit serial number and a FIPS standard-based random number generator, you can use the ATECC108 in consumer electronics, consumables, medical devices, industrial, automation and IP licensing applications that require increased security controls when communicating with other devices or to the Internet.

The ATECC108 authenticates system accessories, consumables and spare parts. Through authentication, you can ensure that only OEM-authorised accessories work with any item of equipment. This device also delivers an overall lower bill of material (BOM) by only requiring one security chip on the accessory side without the need to protect the key storage on the host system side since the host only needs to store a public key. The device is easy to design in, Atmel says, and in many cases will require nothing more than a software upgrade on the host system. According to the NSA, "New techniques have been developed

A 1-chip embedded device protects IP and authorises peripheral connections.

which offer both better performance and higher security than first generation public key techniques. The best assured group of new public key techniques is built on the arithmetic of elliptic curves. 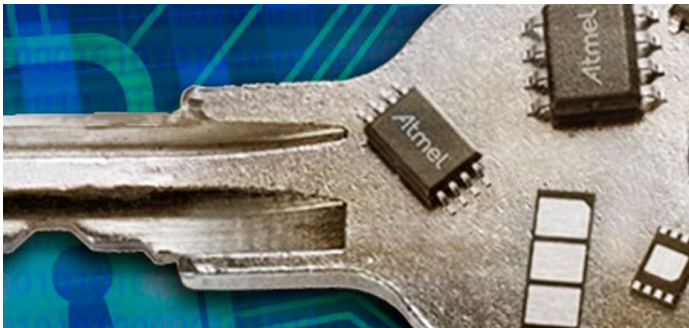[As one] scales security upwards over time to meet the evolving threat posed by eavesdroppers and hackers with access to greater computing resources, elliptic curves begin to offer dramatic savings over the old, first generation techniques."

"In this increasingly connected world, wireless communication is becoming more prevalent making security a very important feature in every design," said Kerry Maletsky, Director of Security Solutions, Atmel Corporation. "There are two fundamental security encryption technologies, symmetric and asymmetric, with the industry rapidly progressing to the latter technology. Atmel's new ATECC108 CryptoAuthentication solution makes this technically difficult shift easier and more cost effective by lowering the overall system cost."

Atmel; www.atmel.com/products/other/cryptoauthentication/default.aspx

LED driver cuts component count, hits volume LED-lighting cost targets

Power Integrations has introduced the LYTSwitch-0 family of highly-integrated LED-Driver ICs for low-power LED bulbs: LYTSwitch-0 is a new series of devices within the LYTSwitch family, intended for cost-sensitive, non-isolated, non-dimmable GU10 bulbs and other space-constrained bulb applications. The earlier, more fully-featured devices in the series – that include dimming – now become " LYTSwitch-4".

LYTSwitch-0 will enable LED bulb manufacturers to hit key price points, PI says, by offering a much smaller total component count, with low-cost components, "13 additional components, when typical designs are using 30-40, and we have seen up to 70". The driver has to account for 35-40% of the cost of the bulb, and in the coming months that total cost will be in the $6-7 region. Also, the company says, to avoid the poor customer experience of CFL lamps, US legislation now specifies a guaranteed minimum lamp lifetime, so manufacturers cannot afford to use low-grade components; a low component-count design is the only option.

LYTSwitch-0 devices feature efficiencies of more than 90% and deliver constant current with better than ±5% regulation in typical applications - "typically 2%", according to a

The new LYTSwitch becomes the entry-level product in PI's LED lamp driver range.

spokesman and "few [other products] even achieve 5%". Power factor is greater than 0.8 at 115 VAC and 0.55 at 230 VAC, meeting all worldwide requirements and specifically ENERGY-STAR V1 draft 3 consumer lighting standards for North America and Ecodesign Directive Lot 19 part 2 for Europe.

The device uses a 700-V FET thus avoiding any need for in-rush current protection; all other applicable protections (temperature, over-voltage, over-current) are integrated, and the chip is self-powered avoiding the need for a complex inductor with multiple windings. Multiple operating modes – buck, buck-boost, flyback and boost – are also supported. Low heat dissipation avoids the need for potting or heatsinking; a typical application schematic does show an electrolytic capacitor on the device output (47 µF/63V) but PI says that configurations with all-ceramic capacitors are possible; and that the low heat dissipation of the drive reduces temperature rise in the lamp and should extend the life of an electrolytic. A reference design, RDR-355, describes a 6W non-dimmable LED driver – see www.powerint.com/sites/default/files/PDFFiles/rdr355.pdf

LYTSwitch-0 IC is sampling in SO-8 and DIP packages; the device costs $0.29 (10,000).

Power Integrations; www.powerint.com/en/products/lytswitch-family/lytswitch-0

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Altera previews its "Generation 10" FPGAs and SoCs

The FPGA vendor has disclosed outline details of its forthcoming Arria and Stratix "10" - for tenth-generation – FPGA product lines. Many of the upgrades in the new product lines – actual release dates for the two series of parts are not yet announced – are enabled by process changes. Arria 10 devices will – initially – be built in TSMC's 20-nm planar transistor technology; Stratix 10 FPGAs and SoCs will use Intel's 14 nm Tri-Gate process (Intel's term for fin-fets) and an enhanced architecture. Among the architectural changes are that, previously, Altera only included embedded processor cores in what it terms low- and mid-range programmable devices. Now, they will become available in high-end parts.

With recent generations of product, Altera says it has been able to keep advancing density figures, but progress in power/performance has slowed, for process reasons: now, the company says it has "broken out" of that limitation and is able to advance on both fronts. Stratix 10 will give you (relative to current Stratix parts) the same performance for 30% of the power: or twice the performance for 30% more power: or 40-60% more performance for today's power levels. These trade-offs are based parameters you can set as a user, on a single device part number. Stratix 10 devices will run at up to 1 GHz clock speeds; they will also include transceivers that will signal (over very short distances, such as between die on a substrate, or between adjacent chips) at 56 Gbit/sec. Referring to these speeds, an Altera spokesman acknowledges, "That's it: after this [anything faster] will have to be optical". Stratix 10 chips will also offer over 10-times the DSP performance, with over 10 TeraFlops, of prior chips. They will include a "hard" processor core; the company will not say what it will be, but notes that, "Our agreement with Intel would allow us to build ARM cores on its [Intel's] 14-nm TriGate process, " adding cryptically, "but you should not read anything into that". Stratix 10 will be "3-D capable" - actually, so-called 2.5-D, permitting logic dice to be mounted side-by-side on a passive silicon interposer to marry them memory and other sub-systems.

More immediate information is available on the Arria 10 family (though still limited details of release dates, as yet) – the mid-range programmable device family delivering both the performance and capabilities of current high-end FPGAs at the lowest midrange power, Altera says; up to 40% lower power compared to the previous family [or] at 15% higher performance. Arria 10 FPGAs and SoCs will have up to 1.15 million logic elements (LEs), integrated hard IP and a second-generation processor system that features a 1.5 GHz dual-core ARM Cortex-A9 processor. Arria 10 FPGAs and SoCs also provide 4-times greater bandwidth compared to the current generation, including 28-Gbps transceivers, and 3-times higher system performance, including 2666 Mbps DDR4 support and up to 15-Gbps Hybrid Memory Cube support. Altera declares support for the HMC concept, saying, "We believe it will become a standard". Generation 10 devices are supported by Altera's Quartus II development software and tools for higher level design flows that include an OpenCL Software Development Kit (SDK), SoC Embedded Design Suite (EDS) and DSP Builder. The Quartus II software will provide Generation 10 FPGAs and SoCs with an 8-times improvement in compile times versus previous generation. The substantial reduction in compile times is the result of leading-edge software algorithms that take advantage of modern multi-core computing technologies – that is, it derives from being able to use more compute resources effectively to run its code.

Early access customers are currently using the Quartus II software for development of Arria 10 FPGA and SoCs. Initial samples of Arria 10 devices will be available in early 2014. Altera will have 14 nm Stratix 10 FPGA test chips in 2013 and Quartus II software support for Stratix 10 FPGAs and SoCs in 2014.

Altera, www.altera.com/Gen10

Android app puts precision power measurements on portables

The Power Viewer Mobile app from Rohde & Schwarz transforms Android smartphones and tablets into high-precision base units for power measurements. The USB-compatible R&S NRP power sensors can now display the measured average power value directly on mobile devices with Android 4 operating system. The NRP range are three-path diode power sensors that cover DC to 110 GHz, with dynamic range up to 90 dB and level range of -67 dBm to +45 dBm. (sensor dependent)

The app, which can be downloaded for free at the Google Play Store uses a feature of the R&S NRP power sensors: their ability to work independently of a specific base unit. The sensors can be connected directly to a PC or laptop via USB. Rohde & Schwarz has now implemented this feature for compact smartphones and tablet PCs. The mobile device must have the Android 4 operating system and support USB host mode. After installing the app, the user only needs the appropriate USB on-the-go adapter to connect the power sensor, and the mobile measuring instrument is ready to go.

The new app provides users with a mobile solution for situations where minimal weight and size of the measuring instrument are essential yet high-precision average power measurements are required; for example, for installing base stations or performing maintenance on microwave link systems. To ensure high measurement accuracy even at low levels, the app can zero the sensor or average the measured values to eliminate the effects of noise. In addition, users can use an offset or S-parameter correction to compensate for attenuators or adapters. The Rohde & Schwarz Power Viewer Mobile app is now available for free at the Google Play store. For more information on installing and using the app, refer to the application note "Using R&S NRP-Z Power Sensors with Android Handheld Devices", www.rohde-schwarz.com/appnote/1ma215

An android tablet becomes an RF power meter

Rohde & Schwarz power sensors, www.rohde-schwarz.com/product/nrpz

BY HOWARD JOHNSON, PHD

SEEK INSPIRATION

1962: I was six, at my grandmother's house, eating pancakes and watching my favorite show on TV. Captain Kangaroo was talking to Mr. Moose about something not quite visible just off the right side of the screen. My grandmother entered the room. She looked at the big console television, tilted her head, and then tweaked the horizontal-position knob. The image shifted a bit to the left, revealing more at the right side. I sat in awe, jaw dropped, gaze transfixed.

When she left the room, I was all over that knob. If you turned it far enough, what would happen? Could you see off the edges of the set? Could you see the cameraman? Could you see yourself? My brain exploded with questions.

1972: I landed a summer job fixing TVs at the local Magnavox dealer. At night, I compared notes with my good friend Glen Collier, who was studying ham radio. Between the two of us, we came to a pretty good understanding of electronics. On the kind of brilliant Saturday afternoon when normal boys should be out-of-doors, Glen and I reversed the connections on the horizontal deflector coil of the new color TV in his family's living room, thus reversing the picture image, left to right. I still laugh when I recall the look on his mom's face, watching the news that evening, taking off her glasses and cleaning them, and putting them back on, vaguely aware that something was wrong with the TV but not sure what.

1982: Professor Martin Graham adopted me as his student. Marty was a rascal and a true genius. He spent the next 10 years passing along his understanding of high-speed electronics and computer architecture. Finding a mentor is one of the best career moves a young engineer can make. I know it sounds quaint, when YouTube and wiki-this and wiki-that can tell you everything you need to know in a minute, but a mentor fills the gap between knowledge and understanding, inspires you to learn more on your own, and opens doors that you never imagined existed.

1992: My experience in analog electronics, digital circuitry, and digital image processing led me to projects in voice mail, robotics, data transmission, video, and Ethernet. Each project taught me new lessons about ringing, crosstalk, ground bounce, and power system design—lessons I began communicating through my writings and public lectures.

That kind of communication creates a whirling vortex of information. The more you communicate, the more people want to talk with you about their difficulties, and the more you learn.

2002: Ten years into the seminar business, I had gotten to know a lot of engineers. The successful ones all have something in common: They think of their career as a system, with inputs and outputs, and arrange the inputs to drive their career in the direction they want it to go. They realize that the more people you know, and the more varied your experience, the better your chances of landing a peach assignment (or surviving a major downturn). Therefore, they pick projects that introduce them to lots of other people and teach them new skills. They seek inspiration.

2012: Having lectured to 12,000 students in seminars all over the world, sold some 100,000 books, built up a program of high-speed digital engineering short courses at Oxford University, raised two wonderful daughters, and had the great pleasure of hearing from engineers like you the technical minutia of thousands of design issues, I began planning the end of my seminar business, and this, my last article for *EDN*. I do not know what the next phase of life will bring, but you can be sure that whenever some new electronic development comes forward, you will find me sitting in front of it, transfixed, gazing with the wonder of a small child.**EDN**

Howard Johnson will teach his last public seminar at the University of Oxford this month. He wishes you the best of success with your next product design and thanks you for your interest in high-speed digital design. If you appreciate his writing, please let him know by making a small donation to his favorite charitable foundation: www.methowmusicfestival.org.

TOP 25
GLOBAL
DISTRIBUTORS

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PLUS+THE
UNBROKEN
CHAIN

How a high-velocity,
dizzyingly complex
supply chain wards off
risk and disruption

TOP 25
GLOBAL DISTRIBUTORS

Every year, EDN's colleagues at EBN magazine conduct a survey of the global Electronics Distribution scene, and of readers's experiences of Distribution and the contribution it makes to their working lives. On the following two pages pages you will find a summary table charting the top global distribution companies by revenue; accompanying this is a sereis of articles that you can find in a special report filed on EDN Europe's web site, here.

Here's Brian Fuller, Editor-in-Chief of EBN, to introduce those articles;

As you'll see from the annual list, not too much changed amid the electronic components distribution landscape in 2012. Some companies lost revenue ground, and some gained—some significantly—but overall it was a flat year.

But the business itself—its internal challenges and opportunities—is wilder than ever, from shifting market and technology priorities, to regulatory and compliance challenges, to counterfeiting, to risk management, to crisis preparedness and management.

The stories in this year's issue help illuminate that and more.

Our overview story, which recalls Ulysses and the Sirens, delves into one of distribution's biggest challenges today: how much to embrace the high-volume, low-margin, and highly volatile consumer electronics business?

Tam Harbert wonders whether any lessons from the Japan earthquake and tsunami and Thailand floods sunk in at all.

Longtime supply-chain editor and observer Barbara Jorgensen ties a neat thread between the two crucial halves of our world: the design chain and the supply chain. What are the conflicts between the two, and how do we resolve them?

And Jennifer Baljko pens an in-depth look at the latest legislation, regulation, and strategy around anti-counterfeiting of components. You can find these and more excellent supply-chain insights in this annual survey. Enjoy!

And what of the specifically European Distribution scene? In a separate survey conducted by publisher UBM, engineers from across Europe gave feedback on their purchasing habits and their preferences when sourcing product from distribution. This table, from that survey, lists the buying habits of the respondents; note that unlike the table overleaf it does not show volume of business but is compiled from answers to the question, "Select up to three distributors that you buy product from." For the same reason, percentages add to more than 100.

The big names in Electronics Distribution continue to add services that extend far beyond "list-it, sell-it and ship-it" to make their offerings useful and attractive to you – for example, read the article in the on-line section, "Tips for design engineers: tapping into online design tools". They'll be trying hard to move up, or maintain, their ranking in these listings over the coming year.

2013 Rank"	Distributor Name	2013 %
1	Farnell/element14	61,0
2	RS Components	52,5
3	Digi-Key	39,9
4	Arrow	28,2
5	Avnet	23,3
6	Mouser	22,4
7	EBV	14,1
8	Future/FAI	10,1
9	Silica	10,1
10	Rutronik	6,1

TOP 25 Global Electronic

2012 rank	2011 rank	Company	2012 total global revenue	2011 total global revenue	% change from 2011	2012 North American revenue	2012 Asia/Pacific revenue	2012 Europe/ Mideast/ROW revenue
1	1	Avnet	25,160.00	26,700.00	-5.8%	10,990.00	7,140.00	7,030.00
2	2	Arrow Electronics	20,405.13	21,390.26	-4.6%	10,641.90	3,836.00	5,927.20
3	3	WPG Holdings	12,397.80	11,111.90	11.6%	N/A	N/A	N/A
4	4	Future Electronics[1]	4,831.00	5,107.00	-5.4%	N/A	N/A	N/A
5		WT Microelectronics	2,800.69	2,365.65	18.4%	N/A	N/A	N/A
6	5	Electrocomponents PLC[3]	2,028.98	1,902.39	6.7%	444.00	N/A	N/A
7	7	TTI Electronics[4]	1,560.00	1,540.00	1.3%	910.00	145.00	503.00
8	6	Premier Farnell[2,5]	1,544.60	1,574.44	-1.9%	N/A	N/A	N/A
9	8	Digi-Key Corporation	1,417.00	1,536.00	-7.7%	974.00	150.00	293.00
10	9	Rutronik Electronics[1]	1,100.75	1,026.82	7.2%	N/A	N/A	N/A
11	10	Mouser Electronics	615.00	582.00	5.7%	386.00	97.00	132.00
12	12	Excelpoint Technology	584.80	489.40	19.5%	0.00	584.80	0.00
13	11	DAC	584.60	564.90	3.5%	574.30	10.30	0.00
14	13	Carlton-Bates[1,6]	384.00	362.30	6.0%	N/A	N/A	N/A
15	14	Dependable Component Supply[1]	334.50	327.00	2.3%	N/A	N/A	N/A
16	16	PEI Genesis[2]	214.00	210.00	1.9%	N/A	N/A	N/A
17	18	Master Electronics	163.00	156.20	4.4%	147.00	N/A	N/A
18	17	Richardson Electronics[2]	149.44	161.03	-7.2%	N/A	N/A	N/A
19	19	Powell Electronics	120.00	120.00	0.0%	N/A	N/A	N/A
20	20	Bisco Industries	116.30	103.20	12.7%	111.80	2.20	2.30
21	21	Flame Enterprises	98.20	101.00	-2.8%	84.40	4.10	9.70
22	22	Electro Sonic	70.00	75.00	-6.7%	68.00	1.00	1.00
23	24	Hughes-Peters	63.00	59.00	6.8%	63.00	0.00	0.00
24	25	Steven Engineering	51.00	49.00	4.1%	45.30	3.00	2.70
25		Hammond Electronics	35.90	37.90	-5.3%	35.9	0.00	0.00

All revenue figures expressed in US$ millions

[1] EBN estimate

[2] Fiscal year sales

[3] North American sales are based on figures at US subsidiary Allied Electronics Inc

[4] TTI acquired Sager Electronics in March 2012

[5] Premier Farnell includes Newark/element14 in North America

[6] Division of Wesco Distribution Inc

Component Distributors

Broadline (b) specialized (s) catalog (c)	Public or private	Headquarters	Website	Products*	Services**
b	pu	Phoenix, AZ	www.avnet.com	s, p, e, i, b, cs, o	l, bom, k, d, si, vmi, t, pk, p, e
b	pu	Melville, NY	www.arrow.com	s, p, e, i, b, cs	l, bom, k, d, si, vmi, t, pk, p, e, as
b	pu	Taipei, Taiwan	www.wpgholdings.com	s, p, e, i, b, cs, o	l, d, vmi, t, p, g, o, bom
b,c	pr	Point Claire, QC	www.futureelectronics.com	s, p, e, i, b, o	l, bom, k, d, vmi, p
b	pu	Taipei, Taiwan	www.wtmec.com	s, o	N/A
b	pu	Oxford, UK	www.electrocomponents.com	s, p, e, i, b, o	bom, k, d, vmi, o
s	pu	Fort Worth, TX	www.ttiinc.com	p, e, i	l, bom, k, vmi
b,c	pu	London, UK	www.premierfarnell.com	s, p, e, l, b, cs, o	bom, k, vmi, pk, o
b	pr	Thief River Falls, MN	www.digikey.com	s, p, e, i, b	d, vmi, p, o
b	pr	Ispringen, Germany	www.rutronik.com	s, p, e, l, b, cs, o	cm, l, bom, d, vmi, pk, p, e
b,c	pu	Mansfield, TX	www.mouser.com	s, p, e, i, b, cs	bom, k
b	pu	Singapore	www.excelpoint.com.sg	s, p	l, bom, d, vmi
s	pr	Wilmington, MA	www.dac-group.com	e, i	N/A
s	pu	Little Rock, AR	www.carlton-bates.com	p, e, i, o	bom, k, d, vmi, t
b	pr	Deerfield Beach, FL	www.dependonus.com	s, p, i, e, cs	bom, k, vmi, t, p
s	pr	Philadelphia, PA	www.peigenesis.com	i, b	k, d
b	pr	Santa Monica, CA	www.masterelectronics.com	p, e, i, b	cm, l, bom, k, d, vmi, t, pk, p
s	pu	LaFox, IL	www.rell.com	p, e, b, o	k, d, vmi, t
b	pr	Swedesboro, NJ	www.powell.com	e, i, b	cm, l, bom, k, d, vmi, t, pk
b	pu	Anaheim, CA	www.biscoind.com	p, e, i, b	l, k, vmi, pk
s	pr	Chatsworth, CA	www.flamecorp.com	e, i	N/A
b	pr	Markham, ON	www.e-sonic.com	s, p, e, i, b, t	l, bom, k.vmi, pk
s	pr	Dayton, OH	www.hughespeters.com	s, p, e, i, b	k
s	pr	South San Francisco, CA	www.steveneng.com	e, i, cs, o	cm, l, k, d, vmi, pk
s	pr	Orlando, FL	www.hammondelec.com	p, e, i, b, o	k, vmi, o

* Products include: semiconductors (s), passives (p), interconnect (i), electromechanical (e), batteries/power supplies (b), computer systems and peripherals (cs), other (o).

**Services include: contract manufacturing (cm), logistics, (l), bill of materials management (bom), kitting and subassembly (k), design services (d), systems integration (si), vendor managed inventory services (vmi), testing (t), packaging (pk), programming (p), environmental (e), ASIC design (as).

BY BONNIE BAKER

Don't be fooled by your amplifier's bandwidth

As we design our SAR-converter analog circuits, we may be tempted to match the voltage-feedback amplifier's data-sheet bandwidth to the bandwidth of our analog signal source. We keep the amplifier bandwidths as low as possible, because faster amplifiers on the board potentially can produce layout headaches. These layout headaches come from putting higher-speed amplifiers in the circuit that are producing fast rise and fall times. The faster signals have the potential to produce EMI signals that other devices or traces on the board can receive, resulting in unexpected noise.

Given this scenario, it makes sense to keep the bandwidth of the circuit's amplifiers as low as possible. With a maximum signal frequency input from dc to 20 kHz, one would think that the required amplifiers would have very low unity-gain bandwidths or a gain-bandwidth product (GBWP).

On the contrary, you need higher-speed amplifiers in the circuit for two basic reasons. The primary reason is to accommodate the lost bandwidth in amplifier circuits that have a closed-loop noise gain greater than one. The other reason is to make sure the bits in your system at the end of the signal path can reliably convert the signal throughout the entire system's frequency range.

Figure 1 shows an example of how the amplifier's closed-loop gain affects the system's overall bandwidth. The GBWP of this amplifier is 20 MHz. The amplifier's closed-loop gain is 10V/V, or 20 dB. In our circuit, we already require an amplifier that has a bandwidth that is 10 times higher than our input signal. You can see this by comparing the intersect of the closed-loop gain ($f_{3 dB}$) with the amplifier GBWP frequency (f_{GBWP}).

The amplifier characteristics shown in **Figure 1** appear to be a perfect fit, but we are looking for the correct amplifier for a 16-bit system.

One sticky point with this circuit is that the amplifier's closed-loop gain is not equal to 20 dB all the way up to 2 MHz. In fact, the closed-loop gain at 2 MHz is 17 dB. This is down 3 dB, which is approximately 70.7% lower than the closed-loop gain, or a 29.3% increase is needed to get up to that curve.

Of course, the circuit's closed-loop gain does not instantaneously change from 20 dB to 17 dB at 2 MHz. Instead, it gradually gets closer to the closed-loop gain curve starting about a decade before 2 MHz. A 20-MHz bandwidth for an amplifier should be good enough, but let's do the math.

This intersection has a simple, first-order attenuation. The correct formula to determine the attenuation back from the 3-dB point toward 0 Hz is $f_1 = f_{3 dB} \times \sqrt{(A_{CL\_DC}/A_{CL1})^2 - 1}$, where A_{CL1} is the target closed-loop gain, A_{CL_DC} is the closed-loop gain at dc, f_1 is the target frequency, and $f_{3 dB}$ is the corner 3-dB frequency of this amplifier system. If you make A_{CL1} equal to 9.9988752, which produces a ~0.0112% error at the full-scale frequency, the bandwidth of the closed-loop system is approximately 100 times lower than $f_{3 dB}$.

With our amplifier circuit, we are not so lucky. We have a 20-kHz signal that we need to increase by 10 times. At the end of the signal chain, we have a 16-bit converter. We find that a 20-kHz amplifier does not work for our circuit. With a signal gain of 10V/V, or 20 dB, the amplifier bandwidth needs to be at least 10 times higher than the signal. We also find that the amplifier bandwidth needs to be at least 100 times higher to maintain ADC integrity. This situation places our amplifier unity-gain bandwidth at 20 MHz. So much for lower-speed amplifiers.**EDN**
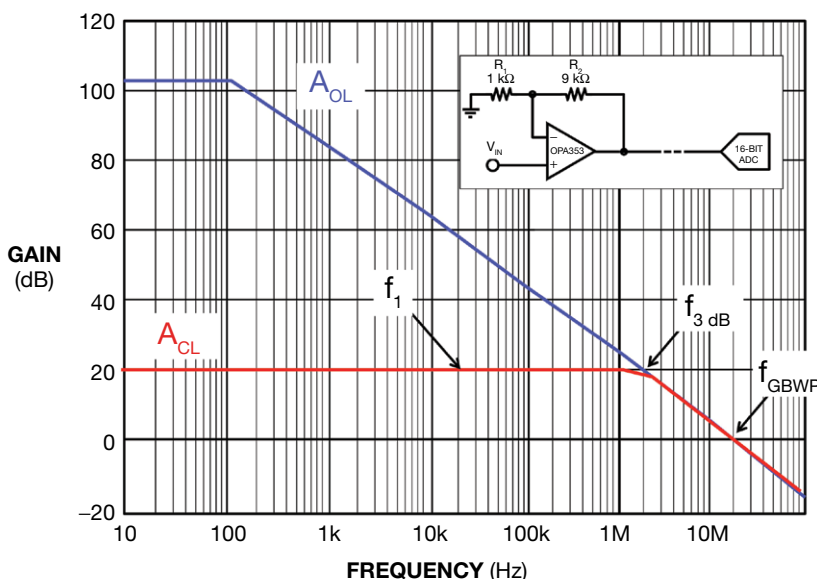
Figure 1 The system bandwidth becomes lower due to the closed-loop (A_{CL}) intercept point with the amplifier's open-loop gain (A_{OL}) and the need to accommodate bit accuracy across the entire frequency range at f_1.

REFERENCE

1 "OPA353 data sheet," Texas Instruments, www.ti.com/opa353-ca.

Bonnie C Baker is a senior applications engineer at Texas Instruments.

EDUARDO OLIVEIRA AND COLLEAGUES, VICOR CORPORATION.

ADVANCED ZVS BUCK-BOOST CONVERTERS FOR MICROPROCESSOR CORE POWER

P roviding power to microprocessor cores continues to present a challenge to power-provision designers; currently, Intel's VR12 specification embodies many of the features that will define next-generation systems. Discontinuous-conduction-mode (DCM), zero-voltage switching (ZVS) buck-boost topology offers numerous advantages and potential gains in efficiency, power density, and performance in this application.

Implementing such a DCM, ZVS, buck-boost voltage regulation scheme will present engineers with challenges that may not typically be encountered with the traditional continuous-conduction-mode multiphase buck topology. In this article, detailed operation of the new scheme is analysed and a control methodology developed to meet the Intel VR12 specification, providing an insight into the design process and showing that the pitfalls can be avoided. A state-of-the art computing power system with outstanding performance can be realised by properly optimising the AC characteristics of each component in the loop, without the need of sophisticated control strategies or dedicated devices.

Using a buck-boost topology from a 48V input followed by a broadband fixed-ratio DC-to-DC converter stage used as a DC transformer is an approach to powering processor core voltage that differs from the more conventional arrangement of a multiphase continuous-conduction-mode buck converter from 12V [References 1-5]. While some of these topologies have offered innovative ways to improve efficiency [Ref. 4, 5], there are cases where using a higher distribution bus voltage (i.e. ETSI 48V) will greatly reduce transmission loss and further improve system efficiency [Refs. 6-11]. The low duty cycle required would make buck conversion directly from these higher bus voltages prohibitive, so a topology that includes a transformer stage is needed. Introducing a transformer stage removes the limitation of having to use a buck converter stage and the benefits of a buck-boost converter can be explored.

There are several challenges in controlling a DCM ZVS buck-boost based topology with an off-the-shelf control IC, beyond those that a more traditional topology will present. First, the modulator gain of the discontinuous-conduction-mode powertrain varies with load [Ref.

12]. Secondly, a ZVS buck-boost topology, when operating near full duty cycle, typically has less "overdrive" ability to transients in both set-point and load. Nevertheless, the potential for reducing transmission losses, as well as the inherently higher efficiency from running closer to full duty cycle and using zero-voltage switching, makes investigation of this interesting topology attractive.

Figure 1 divides the overall converter circuit into two parts; firstly, the discontinuous-conduction-mode ZVS buck-boost converter; and secondly, the DC transformer and passive filter components. The architectural concept is that the buck-boost converter acts as the dependent source while the DC transformer (though a switching component) along with the other filter components can be considered (and analysed) as a passive filter (adding switching noise
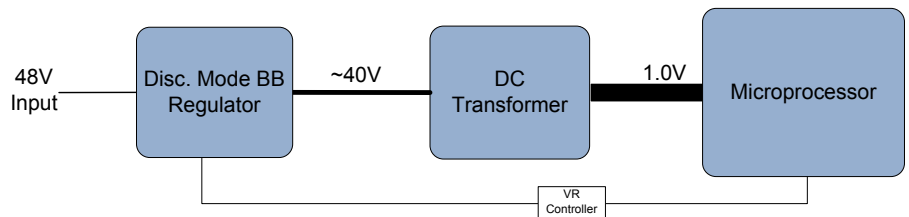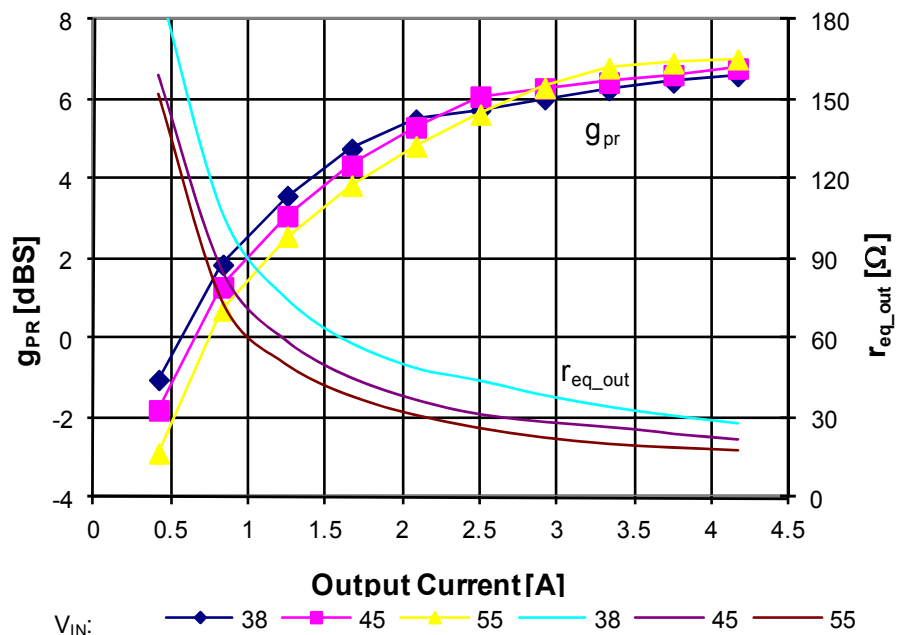
Figure 1. *System block diagram.*

Figure 2. *DC modulator gain and powertrain equivalent output resistance vs. output current, for VOUT = 48V.*
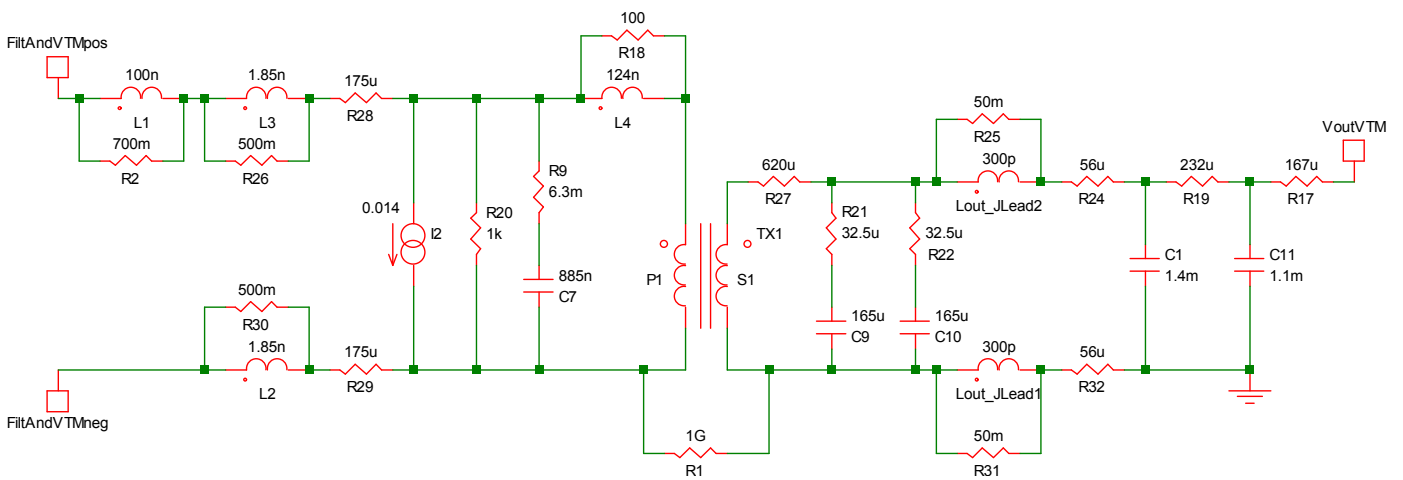
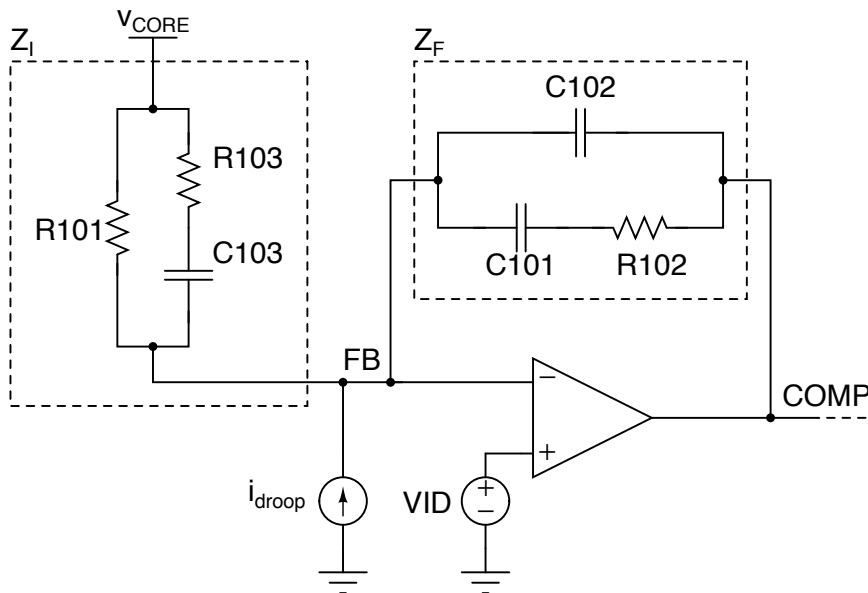Figure 3. *Model of the passive portion of the circuit configuration.*

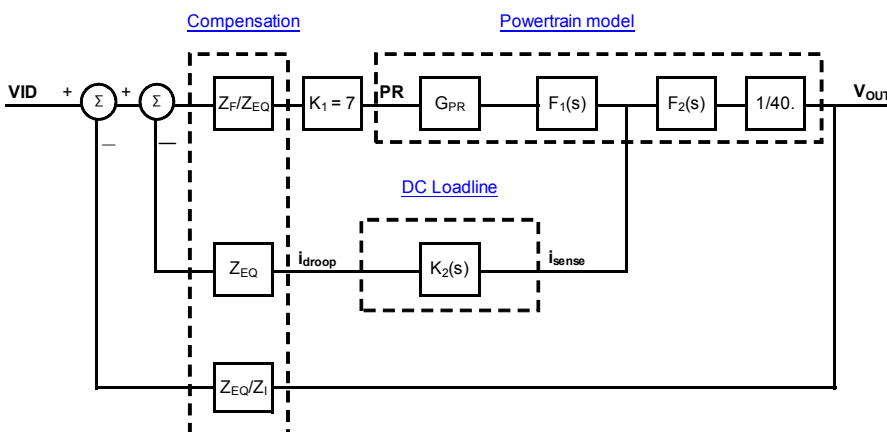Figure 4. *Proposed arrangement for compensation.*

Figure 5. *Model of the entire control system, showing two interacting control loops.*

sources when necessary for analysis). In the system depicted in Figure 1, the discontinuous-conduction-mode buck-boost converter has a load pole at

$$f_{p1} = \frac{1}{2\pi \left(\frac{v_{OUT}}{i_{OUT}} \| \frac{r_{pt}}{N^2} \right) C_{OUT\_eq}}$$

where rpt is the small signal output resistance of the ZVS buck-boost, which also varies with load, VOUT is the voltage at the load, IOUT is the current at the load, N is the turns ratio of the DC transformer, and COUT_eq is the equivalent output capacitance, where the capacitance at the output of the buck boost stage (i.e. upstream of the DC transformer stage) has been multiplied by the square of the turns ratio and added to the load capacitance:

$$C_{OUT\ eq} = C_{LOAD} + N^2\ C_{OUT\ BB}$$

Note that in equation (1), once the load current dominates, as the load increases, the frequency of the dominant pole will also increase. Because this pole is well below crossover, the main effect is to make the buck-boost act as an integrator, though in systems where the modulator gain of the buck-boost is not constant, this leads to a drop-off in gain at light loads.

To optimise efficiency, the discontinuous-conduction-mode powertrain should approach critical conduction at full DC load [Ref. 13]. However, this limits the ability of the powertrain to cope with set-point transients near full load. An accurate analysis over different load conditions is needed, for example in Reference 12. The design described
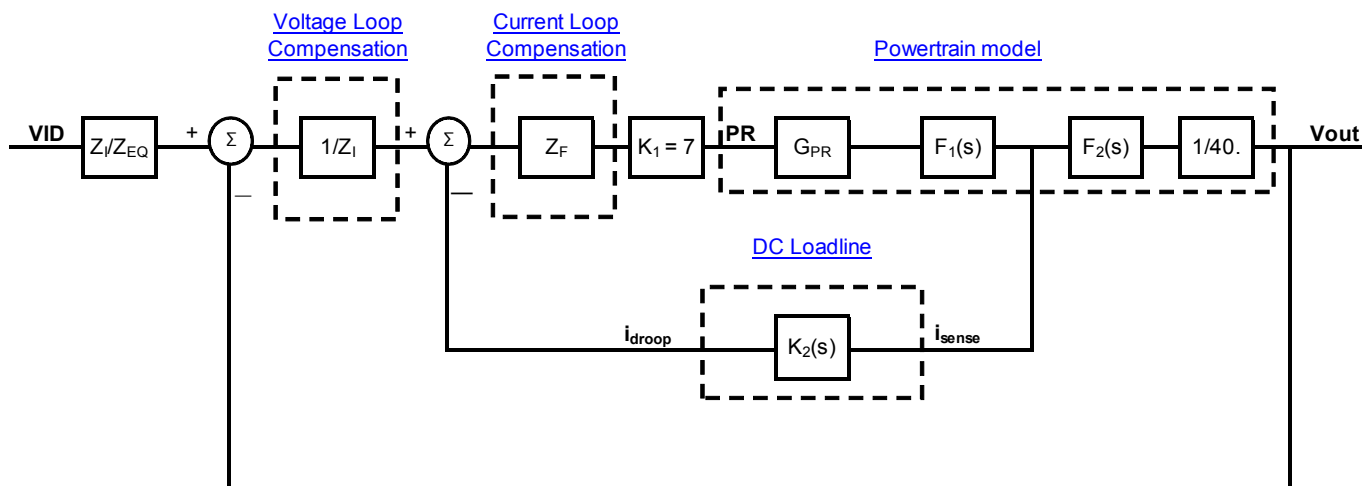
Figure 6. *Control system model, re-arranged to explicitly show the control strategy.*

here is based around a Vicor PRM48DH-480T250A03 ZVS buck-boost converter [Ref. 14]. The resulting modulator gain for the system is shown in Figure 2, and this modulator gain model is used to design the system compensation.

DC TRANSFORMER/PASSIVE FILTER

For the second "passive" portion of the circuit, the model in Figure 3 can be used. This model results in a low-pass system with multiple poles and zeros, for which a pole at 102 kHz dominates. While the system can be treated as a single-pole system up to 300 kHz, the system was analysed with seven state variables, motivated by obtaining accurate gain margin estimates which occur near this frequency.

The control topology employed is the Type III compensator (three poles, two zeros) as shown in Figure 4. In the rest of this article, the network between the output of the compensation and the feedback node (C101, C102, and R102) is referred to as ZF, while the network between the system output and the feedback node (R101, R103, and C103) is referred to as ZI.

In the case of microprocessors with a load-line, there are actually two interacting control loops. As shown in Figure 5, these are the current loop, which controls the output voltage droop proportional to the current, and the outer voltage loop. In the following figures, ZEQ refers to the parallel combination of ZF and ZI.

A strategy for compensation is to first compensate the inner current loop using the first zero and the integrator (ZF), then compensating the phase of the outer voltage loop with the remaining independent zero (ZI) as expressed in Figure
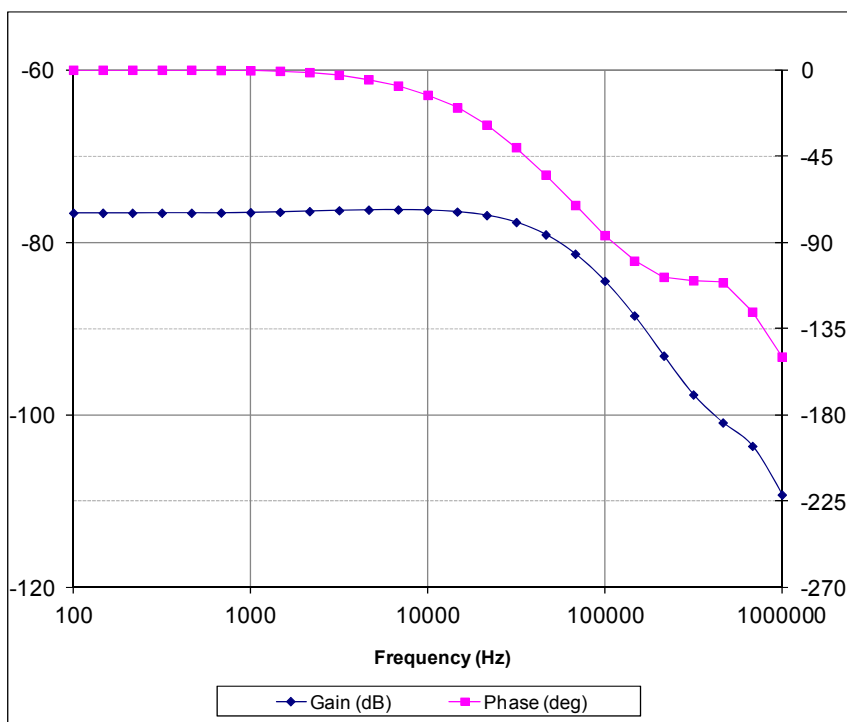

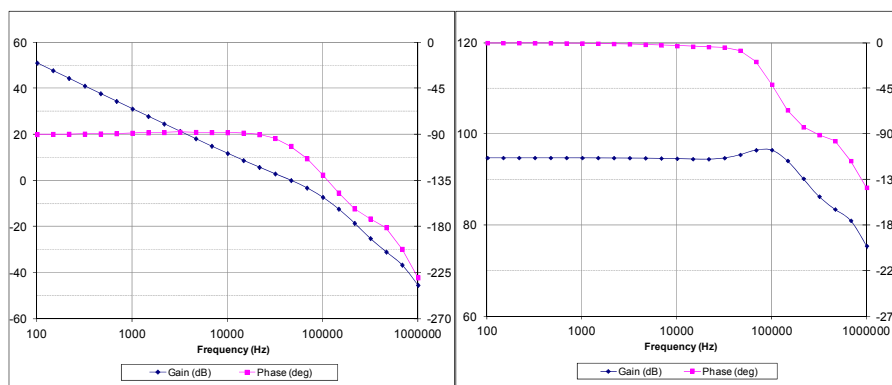**Figure 7.** *Uncompensated loop transmission of the inner (current) loop.*

Figure 8. *Compensated inner loop transmission (left) and closed loop response (right).*
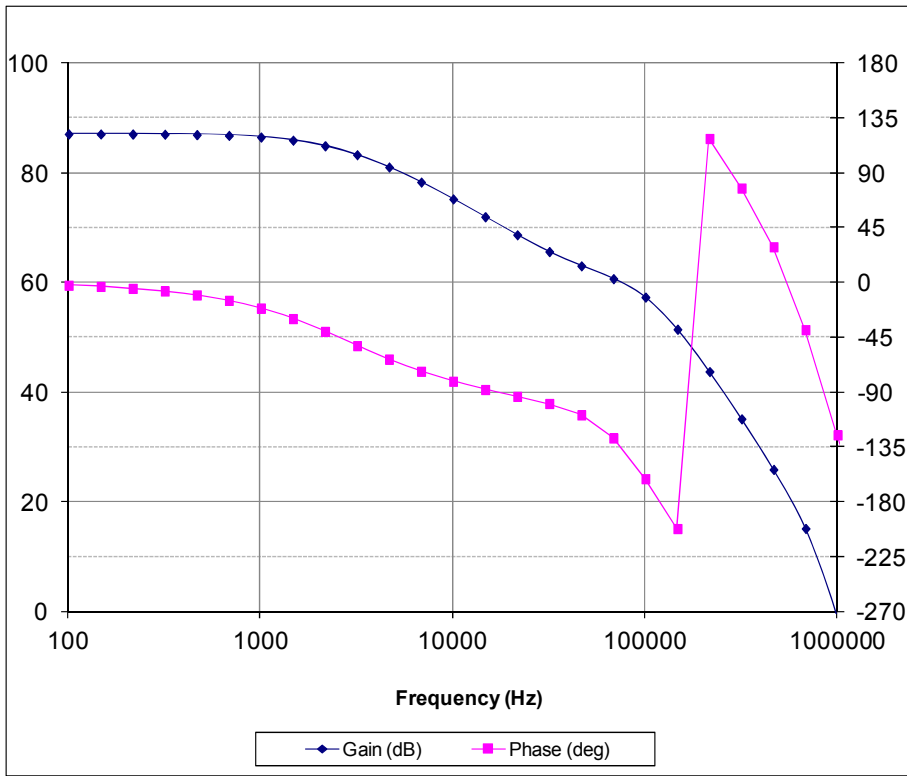
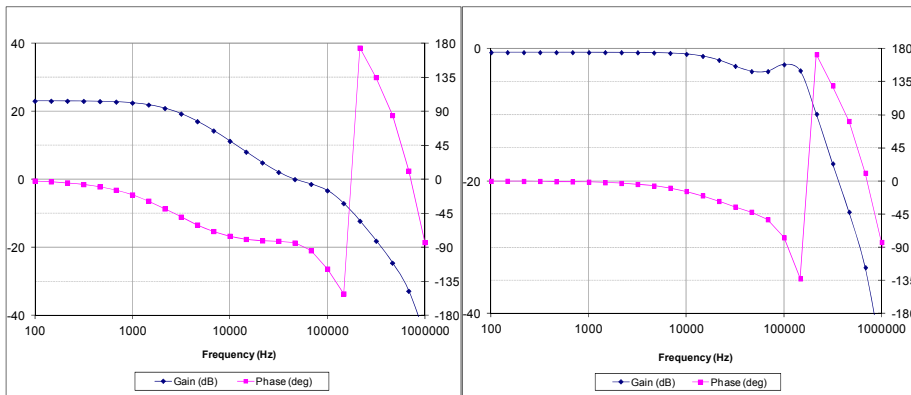Figure 9. *The uncompensated outer (voltage) loop transmission.*

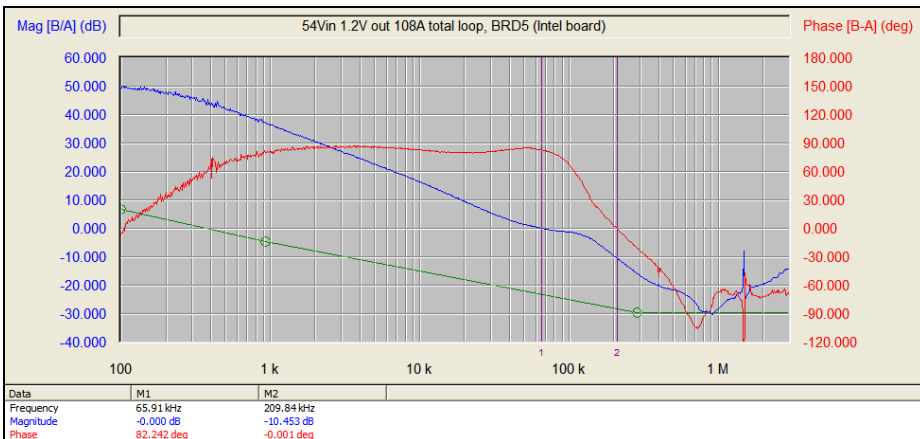Figure 10. *Compensated inner loop transmission (left) and closed loop response (right).*

Figure 11. *Loop response, for a load of 108A.*

6. ZI also contains R101, which sets the load-line and gain of the outer loop. While the loops remain heavily coupled, this method does allow identification of stable solutions, albeit limited in bandwidth by the current loop. Compensation is set with a zero at 30.2 kHz, a pole at 205 kHz, an integrator gain-bandwidth of 14.9 kHz (or, if K1 is included as part of the compensation rather than the plant, the integrator has a gain-bandwidth of 1.04 MHz). The resulting inner loop response is shown in Figure 8.

One benefit of this control method is that one can close the current loop in such a way as to compensate for the load variability of the plant response. As long as the compensated closed current loop maintains its response over the range for which the voltage loop has gain, a non-varying system response is possible, and voltage loop compensation is simplified.

INNER- AND OUTER-LOOP COMPENSATION

The inner loop of this system has an uncompensated loop transmission as shown in Figure 7. Because tuning the gain of the outer loop using ZI is limited, the inner loop should be set such that it has high gain but still remains flat (i.e. the inner loop should have optimised gain margin and phase margin). In designing the compensation admittance 1/ZI, the resistor R101 is predetermined by the load-line. We recommend that this resistance is allowed to determine the loop bandwidth, whereupon the pole-zero pair maximises the gain and phase margin of the system. This method was used to obtain the response in Figure 10, where the zero was placed at 90.4 kHz, and the pole at 1.06 MHz. The model predicts that the outer loop will have a crossover bandwidth of 45 kHz, a phase margin of greater than 90 degrees and a gain margin greater than 10 dB.

In the case of the outer voltage loop, the loop transmission to be compensated can be seen in Figure 9. Note that the gain and phase drop off rapidly at around 100 kHz, therefore achieving a loop response near 100 kHz is difficult.

SYSTEM PERFORMANCE

The system described above was realized using a Vicor PRM48DH-480T250A03 ZVS buck-boost described above [Ref. 14], and a Vicor VTM48EF012T130A01 fixed ratio Sine Amplitude Converter [Ref. 15]. The loop response shown in Figure 11 shows that the phase margin of the outer loop was 82 degrees and the gain margin was

Figure 12. *Response to a 1.05-V to 1.2-V setpoint transient at 108-A load (left) and a 34-A to 165-A load transient (right).*

more than 10 dB, approximating closely to the predicted response, confirming the validity of the model. Across the load range, the experimental system has a crossover between 49 kHz and 66 kHz, phase margin of greater than 75 degrees, and gain margin of greater than 10 dB in all cases.

Microprocessor power specifications have aggressive criteria for setpoint transient response and tolerance band for step responses; in the case of the Intel VR12 specification, these are 20 mV/µsec and ±15 mV, respectively [Ref. 16]. Figure 12 shows examples of conformance of this system to these specifications; in each case, the response exhibits minimal ringing and overshoot.

REFERENCES

[1] G. J. Mehas, K. D. Coonley, and C.R. Sullivan, "Converter and Inductor Design for Fast-Response Microprocessor Power Delivery," IEEE Power Electronics Specialists Conf., 2000, pp.1621–1626.
[2] K. Yao, Y. Meng, and F.C. Lee, "A Novel Winding Coupled-Buck Converter for High-Frequency, High Step-Down DC/DC Conversion," IEEE Power Electronics Specialists Conf., 2002, vol. 2, pp. 651-656.
[3] Li, A Stratakos, A. Schultz, and C.R. Sullivan, "Using Coupled Inductors to Enhance Transient Performance of Multi-phase Buck Converters," IEEE Applied Power Electronics Conf., 2004, vol. 2, pp. 1289 – 1293.
[4] Z. Zhang, E. Meyer, Y.-F. Lui, and P.C. Sen, "A 1-MHz, 12-V ZVS Nonisolated Full-Bridge VRM With Gate Energy Recovery," IEEE Trans. Power Electron., 2010, vol 25. no. 3, pp. 634-636.
[5] Z. Zhang, E. Meyer, L. Yan-Fei, et al, "A Nonisolated ZVS Self-Driven Current Tripler Topology for Low-Voltage and High-Current Applications," IEEE Trans. Power Electron., 2011, vol 26. no. 2, pp. 512-522.
[6] J. Koomey, et al. "A Simple Model for Determining True Total Cost of Ownership for Datacenters." Uptime Institute Whitepaper. Version 2, October 24th, 2007
[7] M. Salato , A. Zolj, D. J. Becker, and B. J. Sonnenberg, "Power System Architectures for 380V DC Distribution in Telecom Datacenters," Int. Telecommunications Energy Conf. (INTELEC) 2012, Oct. 2012.
[8] A. Pratt, P. Kumar and T.V. Aldridge, "Evaluation of 400V DC Distribution in Telco and Data Centers to Improve Energy Efficiency," Int. Telecommunications Energy Conf., (INTELEC) 2007, Sept. 30 2007-Oct. 4 2007, pp.32-39.
[9] P. Yeaman. "Datacenter Power Delivery Architectures: Size and Total Cost of Ownership," Darnell Digital Power Forum, 2007.
[10] A. T. Russell and E. M. A. Oliveira, "Sine Amplitude Converters for Efficient Datacenter Power Distribution," Int. Conf. Renewable Energy Research and Applicat., Nov. 2012.
[11] Mark Murrill and B.J. Sonnenberg."Evaluating the Opportunity for DC Power in the Data Center,": http://www.emersonnetworkpower.com/en-US/Products/DCPower/DC%20UPS/Documents/124W-DCDATA-web.pdf
[12] M. Salato and D. Franzoni, "A Novel Numerical Small Signal Modelling Technique for non-PWM, Discontinuous ZVS Buck-Boost Converter" PCIM Europe Proc., 2011, pp. 1253 - 1258.
[13] M. A. Al-Saffar, E. H. Ismail, and A. J. Sabzali, "Integrated Buck–Boost–Quadratic Buck PFC Rectifier for Universal Input Applications," IEEE Trans. Power Electron., 2009, vol 24 no 12, pp 2886-2896.
[14] PRM48DH480T250A03 Datasheet, Vicor Corporation: http://cdn.vicorpower.com/documents/datasheets/PRM48DH480_250A03.pdf
[15] VTM48EF012T130A01 Datasheet, Vicor Corporation: http://cdn.vicorpower.com/documents/datasheets/VTM48E_012_130A01.pdf
[16] Intel Document, "VR12/IMVP7 Pulse Width Modulation (PWM) Specification," Order Number 397113, October 2011.

Eduardo Oliveira, Adnan Zolj, Maurizio Salato, Paul Yeaman, and Xiaoyan Yu, are all with Vicor In the USA.
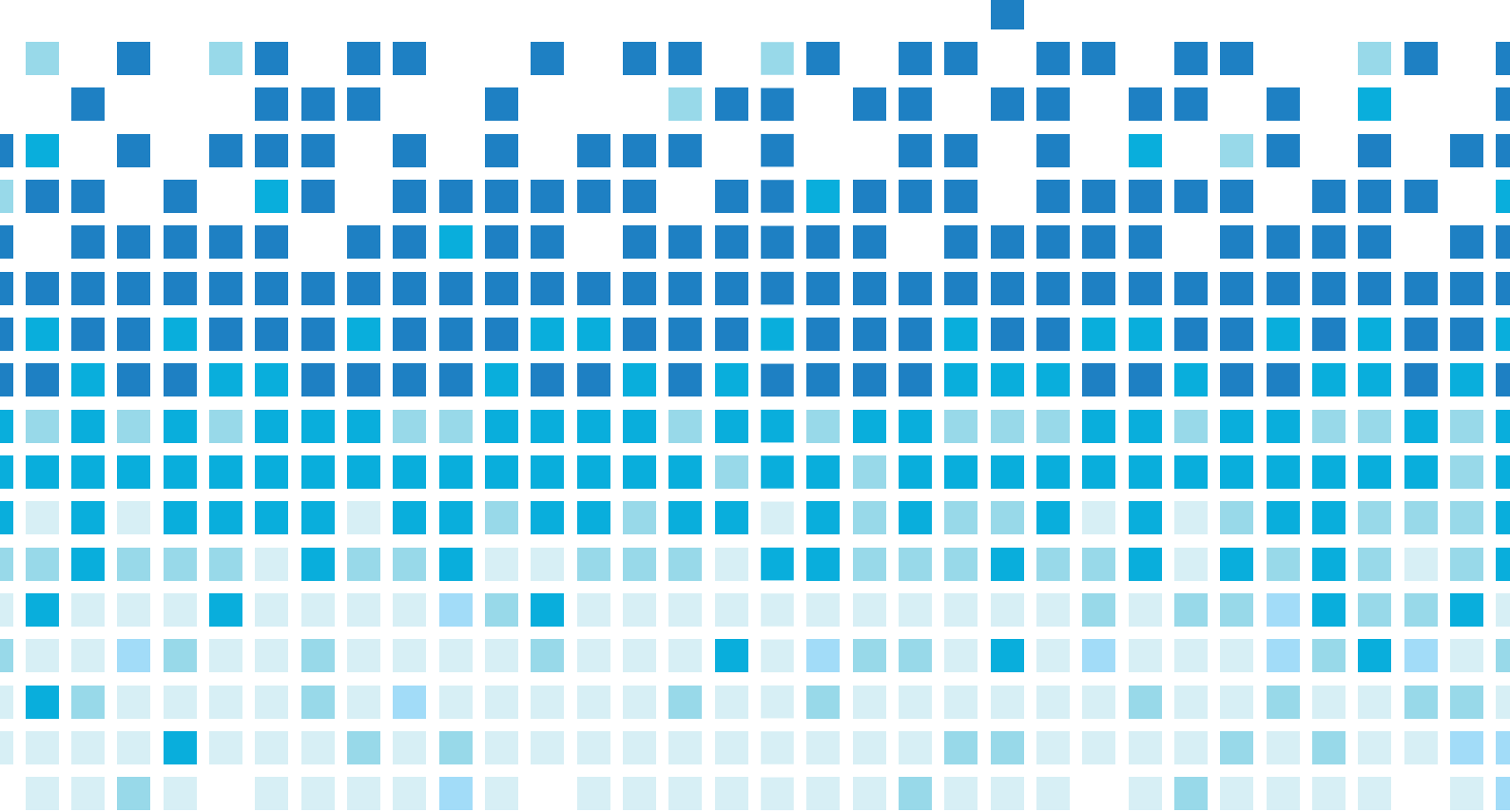
Compensation Attribute	Location in Frequency Domain [kHz]
Integrator Gain-Bandwidth(from Z_F)	1040
Low Frequency Zero (from Z_F)	30.2
High Frequency Zero (from Z_I)	90.4
Low Frequency Pole (from Z_I)	1060
High Frequency Pole (from Z_F)	2050

Table 1. *Summary of compensation parameters for the design.*

COUNTING SQUARES: A METHOD TO QUICKLY ESTIMATE PWB TRACE RESISTANCE

COMPLEX GEOMETRIES CAN BE BROKEN UP INTO DIFFERENT SIZE SQUARES OF COPPER TO APPROXIMATE THE ENTIRE REGION OF INTEREST.

VINCENT SPATARO • BAE SYSTEMS

We often have a need to quickly estimate the resistance of a printed wire board trace or plane without resorting to a lengthy calculation. Although printed circuit board layout and signal-integrity computer programs exist that can accurately compute trace resistance, we sometimes want to be able to make a fast rough estimate as part of the design process. A method that allows us to accomplish this task with very little effort is called "counting squares." Using the method, you can make accurate (within 10% or so) estimates of any trace geometry in just seconds. Once you understand the method, you simply divide the printed wire board area that you want to estimate into squares and then count all of the squares to estimate your total trace or plane resistance.

THE BASIC CONCEPT

The key concept in counting squares is that any size square of printed wire board trace (of a given thickness) has the same resistance as any other size square. The resistance of the square depends only upon the resistivity of the conducting material and the thickness.

This concept can be used on any type of conducting material. Table 1 shows a number of common conductors, along with their bulk resistivity.

For printed circuit boards, the most important material is copper, which is used to fabricate most circuit boards. (Note that aluminum is used to metallize integrated circuit die, and these principles apply there, too.)

Let's start by looking at the square of copper represented by Figure 1. The copper has a length (L), and because it is a square, a width (L). It has a thickness (t), and the current flows through the cross-sectional area of copper (A). The resistance of this copper square is expressed simply as $R = \rho L/A$, where L is the resistivity of the copper (an intrinsic property of the material—0.67 $\mu\Omega$ in. at 25°C).

But notice that the cross-section A is just the length times the thickness. The result is that the L in the denominator cancels the L in the numerator, leaving R=ρ/t. Hence, the resistance of the copper is independent of the square's size. It just depends upon the resistivity of the material and the thickness.

If we know the resistance of any size square of copper and if we can break up the entire trace that we want to estimate into a number of squares, then we can simply add up (count) the number of squares to find the total resistance of the trace!

IMPLEMENTATION

To implement this technique, we need only a table showing the resistance of a square of printed wire board trace as a function of the thickness of our copper. Copper thickness is commonly specified by copper weight. For instance, 1 oz. of copper weighs 1 oz. per square foot.

Table 2 shows four of the most commonly used copper weights and the resistivity of each at 25°C and 100°C. Note that the copper resistance increases with increasing temperature, owing to the positive temperature coefficient of the material.

We now know, for example, that a square of 0.5-oz. copper has a resistance of about 1 mΩ. This is regardless

TABLE 1 BULK RESISTIVITY OF COMMON METALS USED FOR ELECTRICAL INTERCONNECTS

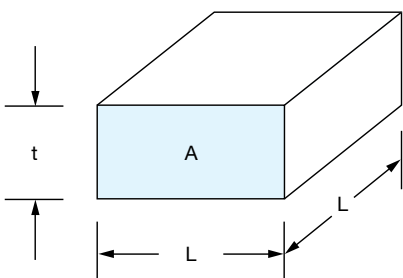| Metal	Bulk resistivity (uΩ-in.)
Aluminum	1.11
Copper	0.665
Gold	0.866
Molybdenum	2.24
Silver	0.642
Tungsten	2.13

Figure 1 *A square of copper can be represented with a length (L) and, because it is a square, a width (L) and a thickness (t).*

AT A GLANCE

↘ Any size square of PWB trace (of a given thickness) has the same resistance as any other size square.

↘ Accurate (~10%) estimates of any trace geometry can be made in just seconds.

↘ The concept works on any type of conducting material.

↘ The resistance of any size square becomes a known quantity once the copper weight is determined.

↘ The resistivity of a corner square counts as fewer squares due to higher current density.

↘ Each via has a finite resistance that must be considered in the overall calculation.

of the size of the square. If we can break up the printed wire board trace that we want to measure into imaginary squares, then adding up all of the squares in series will give us the resistance of the trace.

A SIMPLE EXAMPLE

Let's take a somewhat trivial example. Figure 2 shows a rectangular trace of copper, which is assumed to weigh 0.5 oz. at 25°C. The trace is 1 inch wide and 12 inches long. We can divide this trace into a series of squares, each 1 inch long on a side. There would be 12 squares altogether. Since each square of 0.5-oz.
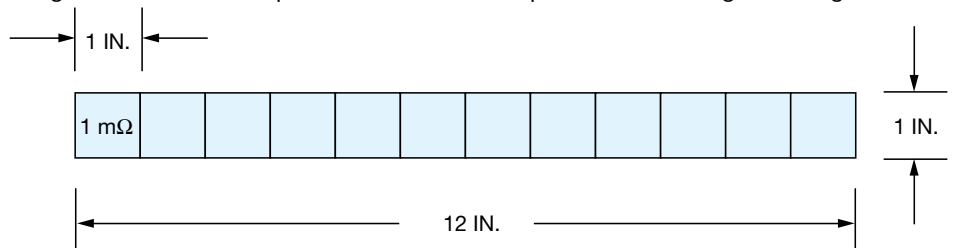

Figure 2 *This example 1×12-in. rectangular trace of copper, assumed to weigh 0.5 oz. at 25°C, comprises 12 squares in series, resulting in a total resistance of 12 mΩ.*

copper is 1 mΩ according to Table 2, and there are 12 squares in series, the total resistance of the trace is 12 mΩ.

WHAT ABOUT CORNERS?

Before we look at a less trivial example to realize the power of this technique, let's look at a few refinements.

The first thing to realize is that, in the previous case, we assumed that current in our square flowed in a straight line along the length of the square, from one end to the other, as illustrated in Figure 3a. However, if current is taking a right-angle turn—for example, in a corner square, as shown in Figure 3b—the situation is a bit different.

Here we see that the current has a shorter path to take in the lower left section of the square than it does in the upper right. As a result, the current tends to crowd in the lower-resistance, lower-left-hand section. The resultant current density is higher in this section than what we see in the upper-right-hand section. The spacing of the arrows illustrates this disparity in current density. As a result, the resistivity of a corner square counts as only 0.56 squares (Figure 4)[1].

Similarly, we can make corrections for connectors that are soldered onto a printed circuit board. Here we make the assumption that the resistance of the connector is negligible compared with the resistance of the copper board.

We can see that if a connector occupies a significant portion of the copper square that is being evaluated, the resistance of that square should be commensurately lower. Three connector-pin configurations and their equivalent square counts[1] are given in Figure 5.

TABLE 2 COPPER RESISTANCE VERSUS WEIGHT

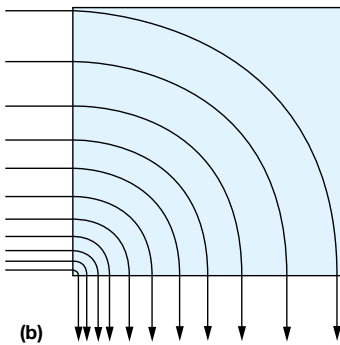| Weight (oz.)	Thickness (mm/mils)	mΩ/square at 25°C	mΩ/square at 100°C
0.5	0.02/0.7	1	1.3
1	0.04/1.4	0.5	0.65
2	0.07/2.8	0.25	0.36
4	0.13/5.3	0.13	0.18

The shaded regions represent the connector pin in the field of copper.

A MORE COMPLEX EXAMPLE

Let's now look a less trivial example to see how we can use this technique. Figure 6a shows a more complex shape that would require some work to calculate its resistance. Our assumption for this example is that we are using 1-oz. copper at 25°C, and current is flowing along the entire length of the trace, from point A to point B. Connectors are placed at each end, A and B.

Using the same technique discussed previously, we can break the complex shape into a series of squares, as shown in Figure 6b. The squares can be any size that is convenient, and different size squares can be used to fill the entire area of interest. As long as we have a square and the weight of the copper trace is known, we know the resistance.

We count six full squares, two squares containing connectors, and three corner squares. Because 1-oz. copper has a resistance of 0.5 mΩ per square, and the current flows linearly through six full squares, the total resistance for these squares is 6×0.5 mΩ=3 mΩ.

Then we add the two squares that have connectors attached, which count as 0.14 squares each (Figure 5c). Therefore, the two connectors count as 0.28 squares (2×0.14). For our 1-oz. copper, this adds 0.14 mΩ (0.28×0.5 mΩ=0.14 mΩ).

Lastly, add the three corner squares. These squares count as 0.56 squares each, contributing a total of 3×0.56×0.5 mΩ=0.84 mΩ. So the total resistance from A to B is 3.98 mΩ (3 mΩ+0.14 mΩ+0.84 mΩ).

To summarize, we have the following:
• Six full squares at 1=6 equivalent squares; two connector squares at 0.14=0.28 equivalent squares; and three corner squares at 0.56=1.68 equivalent squares
• Total equivalent squares=7.96 equivalent squares
• Resistance (A to B)=7.96 squares at 0.5 mΩ per square=3.98 mΩ

The technique can be easily extended to more complex geometries. Once the resistance of a particular trace is known, it is simple to calculate other quantities of interest, such as voltage drop or power dissipation.

(a)

(b)

(c)

Figure 3 *The previous example assumed that current in the square flowed in a straight line along the length of the square, from one end to the other (a). If current takes a right-angle turn in a corner square, as shown, we see that the current has a shorter path to take in the lower left section of the square than it does in the upper right (b).*
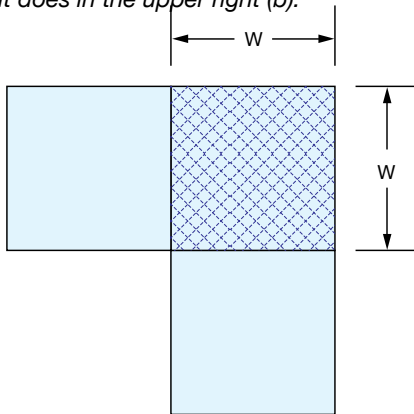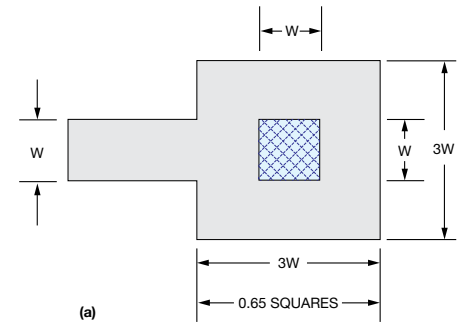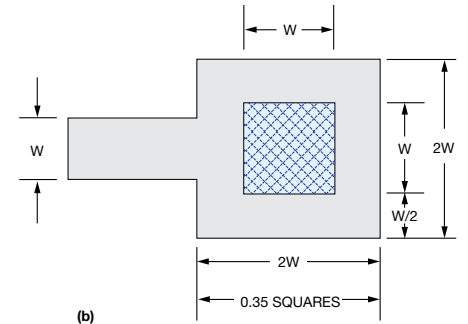

Figure 4 *The higher current density resulting when current flows around a corner means the resistivity of a corner square counts as only 0.56 squares.*

Figure 5 *For the case of a connector soldered onto a board, we make the assumption that the resistance of the connector is negligible compared with the resistance of the copper board, resulting in a lower estimate of that square's resistance. Shown are three connector-pin configurations and their equivalent square counts: equivalent to 0.65 squares (a), 0.35 squares (b), and 0.14 squares (c).*

TABLE 3 RESISTANCE OF COMMON VIA SIZES		
Via-hole diameter (mils)	mΩ 25°C	mΩ 100°C
12	4.3	5.6
14	3.6	4.7
18	2.8	3.6
20	2.5	3.2
24	2.1	2.7
30	1.6	2.1
38	1.3	1.7
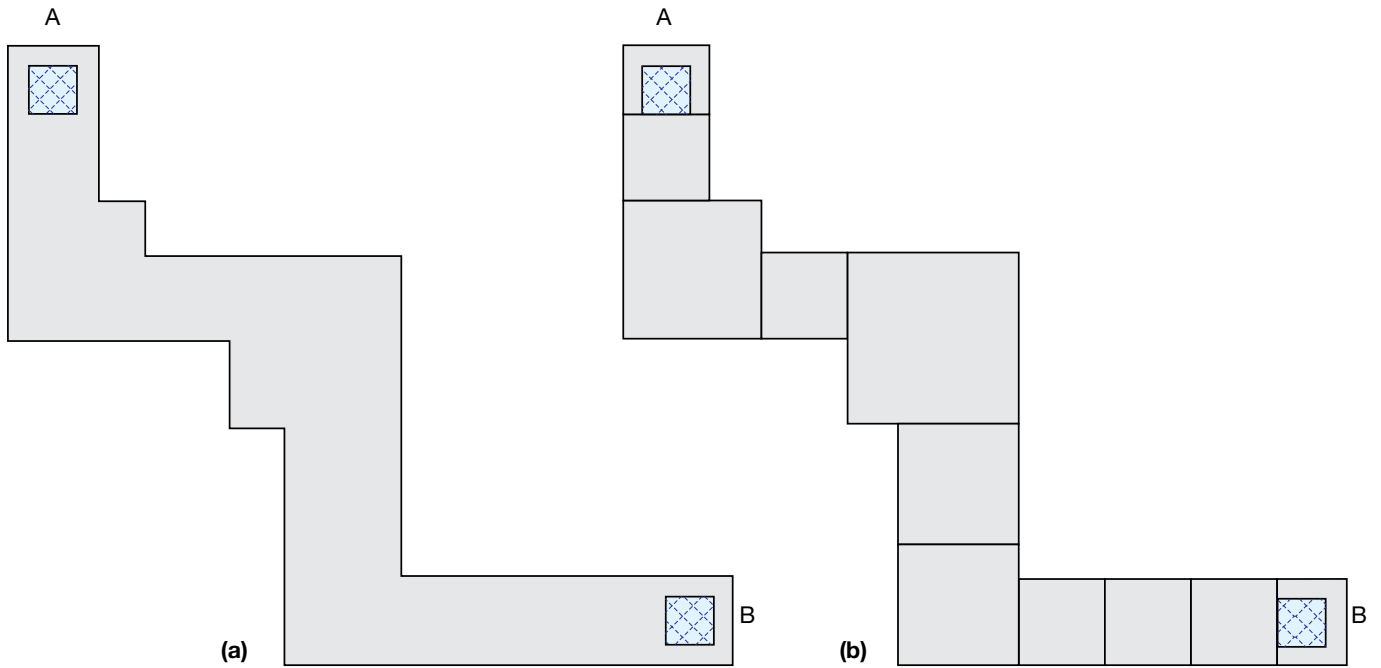
Figure 6 *A more complex shape—an arbitrary shape with connector pads—would require some work to calculate its resistance (a). The complex shape can be partitioned into a series of squares, which can be any size that is convenient (b).*

WHAT ABOUT VIAS?

Often, printed wire traces or planes are not confined to a single layer but continue on a different layer in the stack-up. Vias are used to connect traces together on different layers. Each via has a finite resistance that must be considered in the overall calculation of the trace resistance.

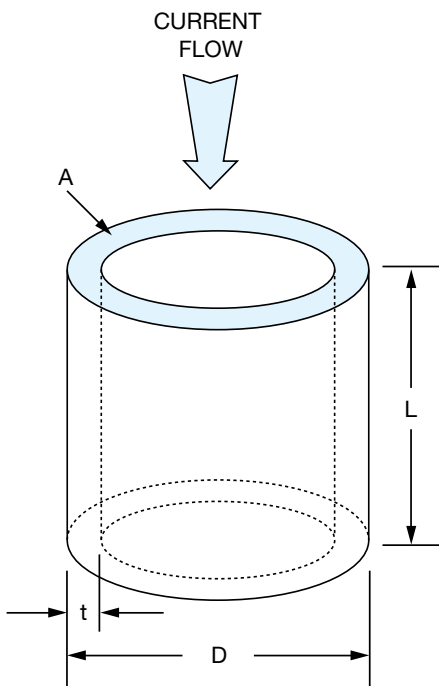Figure 7 *The calculation of via resistance is based on the simplified via geometry shown. Current flows along the length of the via (L), as indicated by the arrow, through a cross-sectional area (A). The thickness (t) is based on the plated thickness of copper inside the walls of the*

Generally, vias constitute series-resistance elements when they connect two traces (or planes) together. Multiple vias are frequently employed in parallel to reduce their effective resistance.

The calculation of via resistance is based upon the simplified via geometry shown in Figure 7. Current flows along the length of the via (L), as indicated by the arrow, and through a cross-sectional area (A). The thickness (t) is based upon the plated thickness of copper inside the walls of the via.

After some simple algebra, the resistance of the via is expressed as $R=\rho L/(\pi(Dt-t2))$, where ρ is the resistivity of plated copper (2.36 µΩ-in. at 25°C). Note that the resistivity of plated copper is much higher than that of pure copper. We can assume that t, the thickness of the plating in the via hole, will generally be 1 mil, regardless of the copper weight of the board. For a 10-layer board, built using 3.5-mil cores and 2-oz. copper, L is about 63 mils.

Based on these assumptions, Table 3 shows commonly used via sizes, along with their resistances. We can easily ratio the numbers up or down for our particular board thickness. Alternately, a number of free, easy-to-use via calculator programs are available online2, 3.

A simple method of estimating the dc resistance of a printed wire board trace or plane was presented. Fairly complex geometries can be broken up into various size squares of copper to approximate the entire region of interest. Once the copper weight is determined, the resistance of any size square becomes a known quantity. The estimation process is then reduced to simply counting the squares of copper.**EDN**

REFERENCES

[1] Jaeger, Richard C; Gerold W Neudeck; and Robert F Pierret (editors), Introduction to Microelectronic Fabrication, volume V, Addison-Wesley Publishing Co Inc, 1988.

[2] Saturn PCB Design Inc, Turnkey Electronic Engineering Solutions, www.saturnpcb.com/pcb_toolkit.htm.

[3] The CircuitCalculator.com Blog, http://circuitcalculator.com/wordpress/2006/03/12/pcb-via-calculator/.

AUTHOR'S BIOGRAPHY

Vince Spataro is a senior member of the technical staff at BAE Systems, Wayne, NJ. He has more than 30 years of experience in the analysis, simulation, and design of commercial/military/aerospace power supplies, as well as experience with a wide range of analog and mixed-signal circuitry. Spataro received a bachelor's degree in physics from Fairleigh Dickinson University (Teaneck, NJ) and a master's degree in engineering physics from Stevens Institute of Technology (Hoboken, NJ). He holds two patents in the power-conversion technology field.

The engineer's mind

With this being the final print issue of EDN, I thought I'd cleave a piece off our recent Mind of the Engineer study to provide a view of your perception of the engineering mind, so this one's all about you: what you think of you, and what you think others think of you. There are some surprises, some affirmations, and of course, some fun twists.

The charts below at first look imposing, but here's how to read them: They show the mean aggregate of pairs of opposing terms, which anchor either end of a scale (from –5 to +5). For each pair of anchored terms, respondents adjust this scale to more accurately express their sentiments about engineers. In the case of Figure 1, your peers were asked to review a series of words or phrases that might describe how they view themselves as an engineer. In the case of Figure 2, they were also asked how others (non-engineers) generally view you, as engineers.

Some quick observations: We generally see ourselves as being risk takers, extroverted, humble, and smart and having a wide range of interests (Figure 2). As we mature in our careers, however, we tend to take more risks, get less humble (More confident, or worse, arrogant?), feel more content (Less ambitious? Settling?), and have a wider range of interests (Done the engineering thing, now what? Retirement?).

For many, Figure 2 will be rather amusing. We think we're risk takers, humble, and ambitious and have a wide range of interests, while we think others view us as risk-averse, borderline arrogant, and not so ambitious and with a very narrow range of interests. Could it be that we're a bit misunderstood? Maybe even feared? For example, we think others view us as smarter than even we think we are! Is that even possible?

Like all studies, you could spend (Waste?) a lot of time analyzing the conditions and parameters of the research: the caveats, biases, sample numbers and source database, culture, conditions, and on and on. Don't do that. Just look at the findings, have some fun with it, take away things that correlate with your experience, and then send this to someone who's not an engineer. See what they think of us!

Add your comments, your observations, and your friends' feedback to this post at www.edn.com/4415695. AS drive in question is a 1-Tbyte Western Digital My Book World Edition, which I used for backing up multiple computers and for music streaming using a Sonos audio network via the shared router. While the device itself was dead, it was not a problem to recover the data from my other external hard drive and back it up to the shiny new 3-Tbyte drive.

I realized when holding the drive just how remarkable it was that a little over 20 years ago I was excited by a 40-Mbyte hard drive, and now here I was holding a 1-Tbyte drive that I just replaced with a 3-Tbyte drive for a scant $170. How did that happen? And why do we take it so much for granted? I had to go inside.

Figure 1 As we grow, we remain somewhat introverted but become a lot less humble (More arrogant?), take greater risks, and have a wider range of Interests.
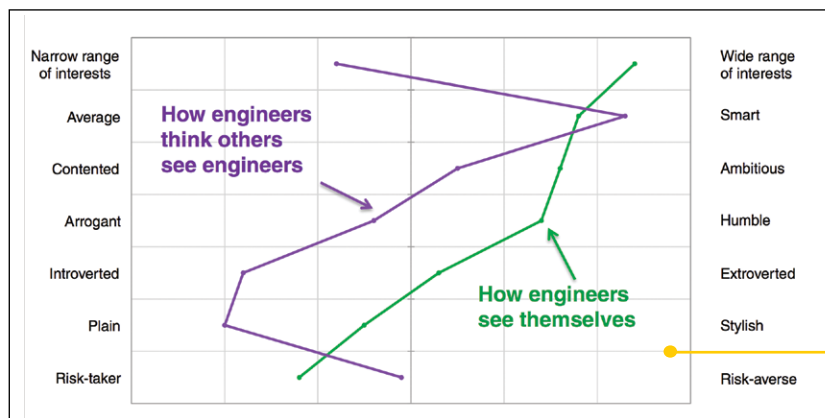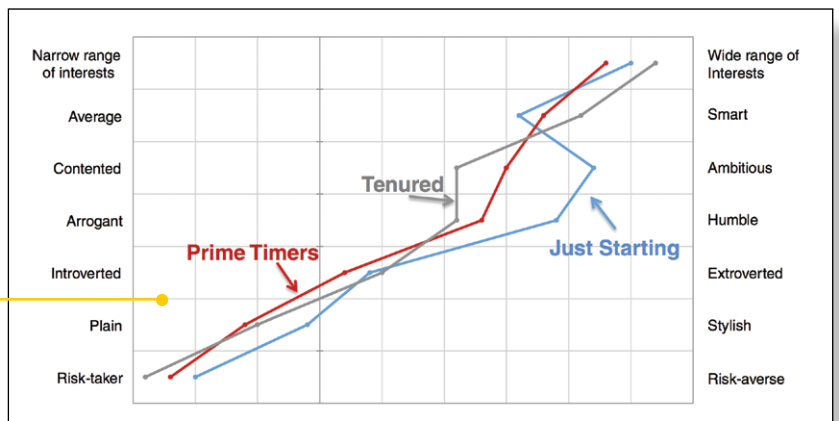
Figure 2 Oddly, we think people view us as smarter than even we think we are. How could that possibly be?

POWER
To The People

By Suzanne Deffree • Executive Editor

There's a growing design trend, some even say there's a revolution brewing, that's beginning to have an impact on the world of design and how engineers go about innovating. Open source—buoyed by the likes of Raspberry Pi, Arduino, 3-D printing, embedded Linux, and strong community knowledge sharing and feedback—is coming to the world of hardware faster than many may think, and with it could come an increasingly democratized approach to the design cycle.

In the world of open source, hardware is years behind software, which is predominantly led by Linux. And there's a key reason for the discrepancy: Hardware is physical, making it more costly and difficult to reproduce. Beyond that, licensing can still be nebulous in some cases, and concerns about IP theft and who profits also hold some back.

But the benefits—including the ability to prototype quickly off of existing, shared work, input from user communities, and low cost or no cost to entry—outweigh the concerns for many design engineers, makers, hackers, or hobbyists, as well as young companies such as SparkFun and Gadget Factory and even more established industry players. These benefits, for many, enhance professional engineering. And open-source hardware is finding its way into designs for everything from fun facial-recognition cameras that add mustaches to photos, to smart watches, to the technology used in the Red Bull Stratos space jump.

The democratization of engineering

When it comes to open source, software is years ahead of hardware. But with encouragement from established electronics-industry players and moves from makers and hackers, engineers could see open-source hardware and an increasingly democratized, community-based approach worked into and enhancing their design cycles.

The definition of what is open source and what is not can be somewhat foggy, varying from company to company or engineer to engineer. According to the Open-Source Hardware Association (OSHWA):

Open-source hardware is hardware whose design is made publicly available so that anyone can study, modify, distribute, make, and sell the design or hardware based on that design. The hardware's source, the design from which it is made, is available in the preferred format for making modifications to it. Ideally, open-source hardware uses readily available components and materials, standard processes, open infrastructure, unrestricted content, and open-source design tools to maximize the ability of individuals to make and use hardware. Open-source hardware gives people the freedom to control their technology while sharing knowledge and encouraging commerce through the open exchange of designs.

What can't be defined, however, are the spirit and passion that open-source hardware ignites in some engineers and developers. Such an excitement is evident at events such as Burning Man and Maker Faire, where creativity, often expressed through open-source hardware, is put on display.

Atmel Corp, for one, has for years been cheering on Arduino, a leading open-source electronics prototyping platform and community. The company continues with its traditional lines but has also begun incorporating Arduino into some products, and showed off

Bob Martin, Atmel's applications manager, hacks a hexbug and puts in an Atmel microcontroller so the bug has intelligence during Maker Faire Bay Area 2013 in May.

AT A GLANCE

↘ Open source can enhance professional engineering and design by expanding the creative pool, offering routes to quick prototyping, and encouraging learning and knowledge sharing.

↘ User feedback from open-source communities becomes invaluable as part of an increasingly democratized approach to design.

↘ It's not just start-ups and independent hackers and makers involved in open source. Established electronics-industry players include Atmel and Texas Instruments.

↘ "Free" and "open source" are different things, with the definitions of open-source hardware and open-source software largely dependent on licensing.

↘ Open source can be profitable, with some open-source hardware companies showing tremendous growth and profit.

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its Arduino development boards based on Atmel AVR UC3, megaAVR, and SAM3X8 ARM processor-based MCUs at last month's Maker Faire Bay Area.

Open-source design wins for Atmel include the Agent Smart Watch, prototyped on an Atmel SAM7X-powered Netduino open-source electronics board. Built by Secret Labs and House of Horology and introduced on Kickstarter, Agent had received more than $850,000 in funding as of press time for this article, a whopping eight and a half times its original $100,000 goal. The smart watch is expected to ship this fall with a finished dual-processor design, using an Atmel SAM4S microcontroller and a tinyAVR.

Eric Weddington, open-source community manager at Atmel, notes that there's been a major increase in the number of companies that are using Ardunio and open-source hardware for prototyping and then further on in product development. "Democratization of engineering: We're already

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seeing that happen," says Weddington. "Arduino has made it so easy to get involved in a complex subject, embedded engineering, which in the past has been the purview of engineers who have a wide range of skills, both hardware and software, in dealing with conflicting restraints and requirements, especially in deeply embedded systems. It has been a kind of very exclusive party of people who can work in embedded systems. But with open-source hardware and Arduino, and open-source software, it has become so easy to use that all of these people who have never had a chance to do [embedded engineering] before can be brought in. That, to me, is the story. It opens up a lot of creativity. People come up with all sorts of uses for the Arduino."

Atmel is not the only big-name player in electronics engineering to broaden its scope and include open source in its strategy. Texas Instruments Inc supports open source through its LaunchPad kits and BeagleBoard and BeagleBone products. BeagleBoard.org—a community where professional developers and hobbyists alike collaborate, showcase projects, ask questions, and offer feedback—launched in 2008 and now averages 50,000 hits per week as one of the most active open-source communities in the industry.

TI's latest addition to the Beagle family is the $45, 1-GHz BeagleBone Black open-source Linux computer, released at DESIGN West in April and based on the company's 1-GHz Sitara AM335x ARM Cortex-A8 processor. More than 30 plug-in boards, which the Beagle-Board.org community calls "capes," are compatible with BeagleBone Black, and more capes are expected. Integration of BeagleBone Black with these capes—such as 3-D printers, a DMX lighting controller, a Geiger counter, a telerobotic submarine, and LCD touch screens—so far has received positive reviews.

Black has even gotten a thumbs-up from Limor "Ladyada" Fried, recently named Entrepreneur magazine's Entrepreneur of the Year in the established-engineer category for her work as a longtime supporter of open-source design and founder of Adafruit Industries, which is selling the Black platform.

Jason Kridner, co-founder of Beagle-Board.org and TI software architecture manager for embedded processors, points out that there's a difference between free hardware and open-source hardware. "You can have things that are freely available, but there can still be things in the licensing terms that restrict where you can go and what you can do

The Agent Smart Watch, prototyped using an Atmel SAM7X-powered Netduino, offers two-way communication to smartphones, wireless charging, and long battery life.

with it. Whether or not it's open source is really just in the license terms, not in how much you pay for it or don't pay for it," he explains. "Sometimes there are things where you need to contribute back, and that's an important part of growing the community. But for the most part, we [at TI] try to make sure you can do what you want, and for certain that you can do what you want with the hardware."

Contributing back often comes in the form of feedback in such open-source communities. "The most valuable element that the community lends is the improvement cycle, the feedback cycle," says Chris Taylor, an engineer at 10-year-old SparkFun Electronics, an open-hardware company that's growing quickly with more than 130 employees and 450 original products.

"In our case at SparkFun, when we post a design's code online and someone takes that code, uses it, and finds an improvement or an error, we can make the improvement immediately, thanks to the community," Taylor adds. "If the hardware has an improvement to be made, that is put as a comment on the product page as a forum. Because it's open source, anyone can make an improvement, and when SparkFun sees it, they put the improvement into the revision cycle. So the next version of that product is going to be better because of that community. That feedback, coupled with agility to turn out a new product, is the benefit to having the open-source

community."

Gert van Loo, who developed the prototype of the extremely popular Raspberry Pi board and created the Gertboard, an IO expansion board for the Raspberry Pi with a lot of flexibility, points out that the Pi would be nowhere without community feedback. The Pi was created to spur creativity and computer science and engineering learning—a goal it has achieved tremendously—but van Loo notes that the low-priced board never would have achieved this without nourishment from the open-source community.

"The plan has always been from the beginning to throw a lot of boards into the community, and then quite a lot of the development for the education, support, software, and drivers, all that stuff that you needed, would come back from open source again. That was always the idea," he says. "At the beginning, it was very clear that the final target was education, but the first batch that went out into the world we knew would definitely not be going into education. That would have been a disaster. This line of development, envisioned by [Eben Upton, founder of the Raspberry Pi Foundation], was the initial target we followed."

SKILLS, BUT CAN THEY PAY THE BILLS?

While all of this giving back is wonderful knowledge sharing, the big question to some engineers then becomes one of income and payment for IP. How will the individuals who participate in these communities benefit if they do so
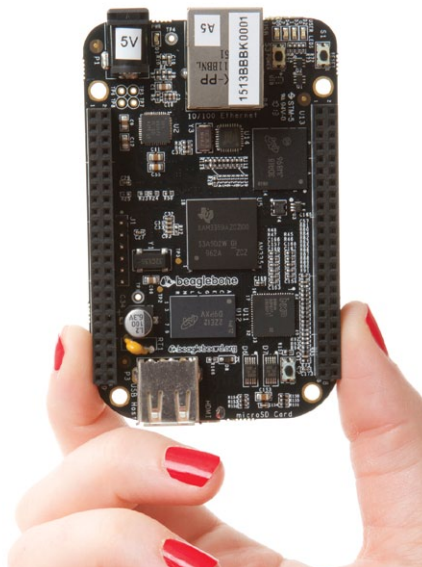
The $45 BeagleBone Black is a credit-card-sized, Linux computer open-hardware and -software development platform.

for free? Who's getting paid?

"The Linux foundation has good stats in this," says Brad Dixon, director of open source and tools solutions at Mentor Graphics Corp, which plays in open source with its Embedded Alley runtime Linux and Android offerings and Code-Sourcery GNU-based toolchains for embedded development. "It's a myth that people think the Linux kernel is created by hobbyists at home. The overwhelming majority of people who contribute to Linux do so because it's their job and they get paid to do it. People contribute because they get paid.

"Often you see people contribute because it benefits them. There's an issue they've struggled with, and they know that if they can make the improvement they won't have to fight it again. Or, in many cases, they want to get into a field and this is their way to audition, to be part of a global talent pool. We have a number of engineers [at Mentor] that we've met along the way in the open-source world that we've [invited] to come work for us."

When it comes to open source as a base for a start-up business, things can get tricky, say the founders of Gadget Factory, the four-year-old company behind the Papilio FPGA platform, that is quickly making a name for itself.

"Without open source, none of the products we've made so far would even exist. That's why all of our boards are open source. We want people to be able to build on top of what we've done," says founder Jack Gassett.

But Gassett believes there needs to be another revision of the open-source-hardware (OSHW) license to allow for better commercial licensing. "At the end of the day, we live in a capitalistic society. Open source is sometimes at odds with that," he explains. "We are running a business, and our intention is to build the business and make money. We continue to gather resources so that we can continue to invent and bring new products to the market, but neither one of us are setting out to be millionaires."

Adds his partner, Kalesh Weaver, a former hacker, "Open source isn't saying don't make money; it's saying the information is free. Every successful open-source community has a successful side commercial community, usually made of the developers who first started working on it and know it best. Don't those people deserve to be paid to keep working on it?

"Look at the Internet and freedom of information. It's changing cultures across the world. And that's what the

hackers have said all along: We can't stop it; just find your niche and do it well, and someone will compensate you for it."

As a group, the OSHWA is reviewing licensing as part of exploratory meet-ups it calls "document jams," where active OSHW developers gather to discuss and look for ways to make more standardized open-source design documentation. This includes unclear licensing and fear of infringement on IP rights that the group believes may discourage people from producing documentation. Says t he OSHWA, "Documenting involves reuse of content from other sources. If people do not understand IP licenses or have little understanding of their own IP rights to use content, they may be afraid to contribute documentation. A clear how-to on open hardware documentation IP issues, as well as a legal support framework, can mitigate this."

That's not to say that closed-source hardware doesn't have its own set of licensing and IP issues, nor to suggest that open-source hardware design immediately comes with licensing and IP problems.

"You always have to understand the license under which you acquire intellectual property. Whether it's an open license or closed license, you have to understand what you are getting," TI's Kridner says. "An open nature doesn't necessarily generate a problem; you just always need to be aware of the terms under which you acquire intellectual property."

NEAR-TERM LIMITS,
BUT WITH LIMITLESS POTENTIAL

Clearly in the near future, engineering won't jump to entirely open-source hardware design, just as all software design has not become Linux based. But there's tremendous potential ahead for enhanced design as more individual engineers and companies embrace it.

"There's no such thing anymore as hobbyist hardware," van Loo says. "Processors and PCB electronics are no longer simple to develop. That's a reason why open-source hardware is gaining place. A high-end processor is not trivial to design
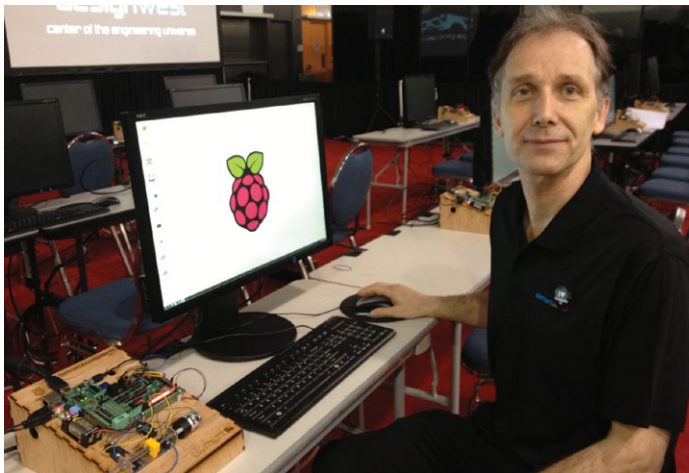
Gert van Loo sets up a Gertboard at a workshop during April's DESIGN West 2013 event. Everyone who attended this session received a free Gertboard provided by Newark element14.

anymore. On the other hand, for a big company it's peanuts compared to what they spend on marketing and everything else.

"[Open-source hardware] makes it easy to select a processor, try it out, and a lot of amateurs can use it, but it only goes so far," he adds, cautioning against the use of current open-source hardware in areas that have to be absolutely safe and excessively tested, such as automotive and military.

Still, open-source hardware and its simple systems are part of a broader change. "Open-source hardware is just one component of the democratization of manufacturing overall," says TI's Kridner. "There's an outburst of maker spaces and hacker spaces. There's been the development of tools around laser cutters and 3-D printers, and all these things that you need to do professional-grade manufacturing seem to be accessible to the average person. That's really democratizing manufacturing."

Indeed, when companies such as Cooking Hacks can offer an Arduino-based 3-D printer kit for around $850 that allows for inexpensive and quick production of mechanical parts for prototyping (see page 14), there's a potential shift in design methodology.

"We're getting closer and closer to being able to e-mail someone a design and print out a cell phone," says SparkFun's Taylor. "People are taking closed-source designs and replicating them, scanning them into 3-D files, and printing them out on 3-D printers."

But that's not coming tomorrow, or the day after, for that matter. And, although open source will allow for more amateurs to engineer, the role of the professional engineer only enhances.

"Democratization of engineering, overall, really enlarges the pool of creative ideas that can get to market, but we also have to differentiate between the types of ideas that can get to market without the formal engineering, the more professional engineering," says Atmel's Weddington. "Blinking a light is always mentioned in embedded systems as the 'hello world' application. It's easy to do something like that. But you really need the professional engineering background if you are going to develop something like a medical device or avionics on a plane. I don't see the democratization of hardware taking away from the traditional professional engineering group at all; I just see it as adding to it."**EDN**
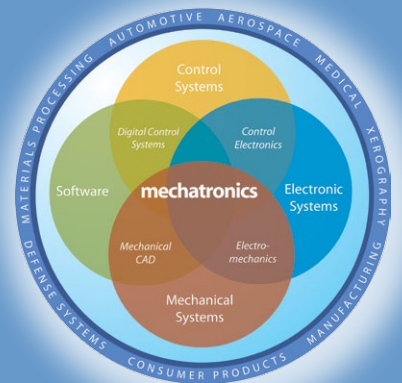
Managing complexity and reducing risk

High-risk technologies exist everywhere. How should engineers respond?

By Kevin C Craig, PhD

This column, over the years, has had the theme that human-centered, model-based design is the most direct path to insight and innovation. The innovation diagram (Figure 1) shows the added importance of viability and sustainability, and also introduces the need to manage complexity. We are now surrounded by high-risk technological systems in all aspects of our lives. Is the potential for catastrophic failure inherent in the system itself, or in the way the system was designed? Charles Perrow, in his most relevant book, Normal Accidents (Princeton University Press, 1999), addresses this question and develops an explanation based on system characteristics.

Systems are fundamentally made up of components or parts. A functionally related collection of components forms a unit. An array of units forms a subsystem. Subsystems come together to form the system. An accident is a failure in a subsystem, or the system as a whole, that damages more than one unit, and in so doing disrupts the ongoing or future output of the system.

What kinds of systems are prone to system accidents? To answer this question, you need to consider two concepts: interactiveness and coupling.

The notion of baffling system interactions is increasingly familiar to all of us. Interactiveness is not a problem if the interactions are expected and obvious. However, components sometimes have a common-mode function in that if one fails, other modes fail. The situation then gets more complex. Ironically, complexity is often added to a system to reduce common-mode failures. Proximity and indirect information sources are two other indicators of interactiveness. Simple, comprehensible interac-

tions are predominant in all systems. But as the complexity of a system increases, the probability that baffling, unintended interactions exist increases dramatically. This classification is fuzzy, and systems must be characterized in terms of the degree of either quality. Complex systems are not undesirable. They typically are more efficient with less slack, less underutilized space, less tolerance of low-quality performance, and more multifunction components. But they also could have the potential for catastrophic failure.

The second concept to consider is coupling. Tightly coupled systems have more time-dependent processes, the sequences are invariant, and there is little slack. The overall design of the system allows only one way to reach the goal. Coupling is particularly germane to recovery from inevitable component failures. In tightly coupled systems, the buffers, redundancies, and substitutions must be designed in; they must be thought of in advance. In loosely coupled systems, there is a better chance that expedient, spur-of-the-moment buffers, redundancies, and substitutions can be found.

The world of systems can be organized according to two largely independent variables: loose versus tight coupling and predictable versus baffling interactions. Loosely coupled, predictable systems include assembly-line production and most manufacturing, while tightly coupled, predictable systems include rail transport and dams. Loosely coupled, complex-interaction systems include R&D firms and universities, while tightly coupled, complex-interaction systems include nuclear plants, aircraft, and space missions.

There are no answers here. Engineers must manage complexity and prevent catastrophic failures. Interactiveness and coupling are two concepts that should aid engineers in accomplishing that goal.**EDN**

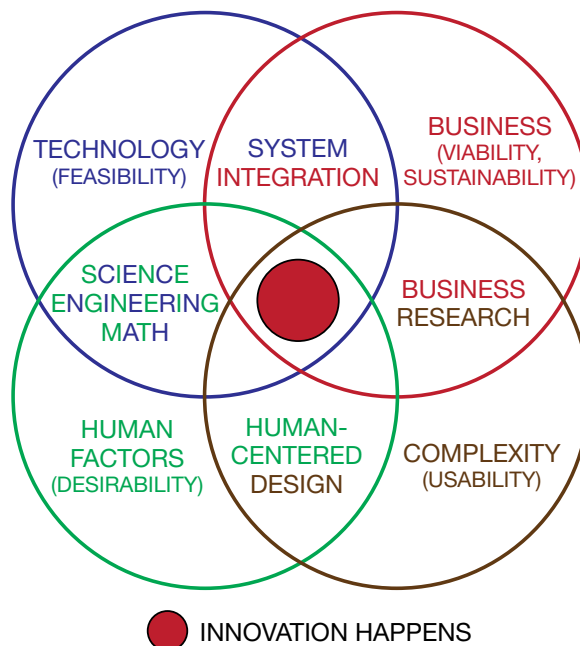**Figure 1** *The innovation diagram shows the added importance of viability and sustainability, and also introduces the need to manage complexity.*

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READERS SOLVE DESIGN PROBLEMS

Derive an efficient dual-rail power supply from USB

RO Ocaya, University of the Free State, Phuthaditjhaba, South Africa

When designing low-power USB circuits that require power-supply voltages other than 5V, you must decide whether to use a separate battery or a physically small mains-based power source. The problem is particularly troublesome if the circuits to be powered require dual rails greater than 5V, such as instrumentation amplifiers based on operational amplifiers, or must be run on portable computers, such as laptops.

The USB 2 standard specifies the power requirements of a connected device as either low power if it consumes at most 100 mA, or high power if it consumes up to 500 mA. The origin of the circuit described here is the design of a thermoluminescence (TL) instrument for which the microcontroller, the USB-interface controller, and 10 operational amplifiers are all powered from a standard USB port as a low-power device. The operation of the device requires high-efficiency performance with little noise pickup and keeping radio-frequency emission from the system as low as possible. The circuit was simulated before being built and verified and then used in the TL system. The design is attractive because its use of common components improves repeatability while keeping costs extremely low.
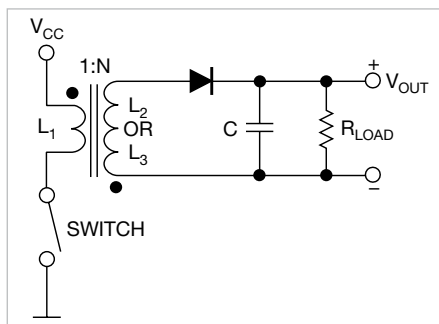
Figure 1 *This basic flyback converter pumps magnetically stored charge into filter capacitor C when the switch opens.*

The operation is based on the flyback concept (Figure 1), where a small transformer is driven at 115 to 300 kHz generated by a pulse-width-modulated 555 astable circuit. The high frequency of operation allows the overall size of the circuit to be kept small while delivering relatively high power output with good regulation, and allows easier output filtering for low ripple.

In the actual circuit, you implement the switch using a MOSFET. In Figure 1, the diode is shown forward biased for positive VOUT. Reversing the diode direction and the polarity of one transformer winding gives a negative VOUT. The circuit operates in three distinct phases. In phase one, the switch is closed and energy is stored in a magnetic field due to current flowing in the transformer primary. The diode is reverse biased, and no current flows in the secondary.

In phase two, the switch opens, the diode becomes forward biased, and the energy is transferred from the magnetic field into capacitor C. In phase three, with the energy dump completed, any residual charge stored on the switch drain-source capacitance is completely discharged. The cycle is then repeated.

To better explain the operation of the circuit, it is easier to presuppose that just prior to time t=0, the filter capacitor is already charged to the nominal output voltage and that the current through the primary windings of the transformer is zero. At t=0, the switch closes and a current starts to flow through the primary winding. This will induce a voltage across the secondary winding with a polarity as indicated. Since the diode is reverse biased, no secondary current can flow and the secondary winding is effectively open-circuit. The primary side of the transformer behaves like a simple inductor. As a result, the primary current increases linearly according to the following equation:

$$I = \frac{V_{CC}}{L_1} t.$$

During the time the switch is closed, the voltage induced across the secondary windings is nVCC. The diode must therefore withstand a minimum reverse voltage of (nVCC+VOUT). At a given instant later, the switch is opened. In the practical circuit, this corresponds to the MOSFET's being turned off. Suppose that the current in the primary winding at that instant is IPK. The magnetic energy stored in the inductor is then equal to

$$E = \frac{1}{2} I_{PK}^2 L_1.$$

Due to the flux linkage between the primary winding and the secondary winding, with the primary circuit open, the inductor's stored but collapsing magnetic field induces a voltage at the secondary side high enough (>VOUT) to forward bias the diode. The initial value of the current will be I2=IPK/n. During the time that the diode is forward biased, the voltage across the secondary winding will equal (VOUT+0.7). This can also be seen as a transformation of the primary-side voltage down to VOUT/n. The switch, therefore, has to withstand a voltage of effectively
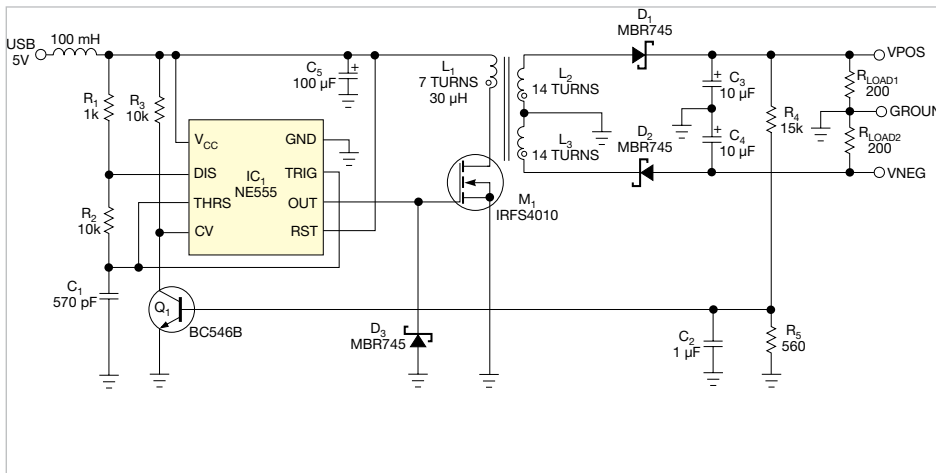
$$V_{REVERSE} = \left(V_{CC} + \frac{V_{CC}}{n} \right)$$

when it is open. This last equation highlights the main advantage that the flyback converter has over the boost converter of comparable input and output voltages, namely the reduced voltage the switch must handle when it is opened. In effect, the voltage during the "off" phase is transformed down to a value determined by the trans-

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Figure 2 *In this complete circuit, you can use many alternatives for M1, Q1, and the Schottky diodes.*

former winding turns ratio. This allows a MOSFET with a much lower breakdown voltage to be used. Additionally, in the boost-converter topology, the diode must handle both the high "on" current and a high reverse voltage in the "off" phase. In the flyback converter, the diode at the secondary side has to withstand only a high voltage while the current is low (IPK/n). This permits the use of a diode with smaller capacitances that results in higher switching speed with the consequence of reduced energy losses and an increased efficiency. Although it is beyond our current scope, you can calculate the output voltage by equating the amount of energy input in L1 to the energy transferred to the load, RLOAD. In steady state, the output is related to the duty cycle, D, of the switch and the frequency at which the switch is operated; that is, the open-circuit output voltage is given by

$$V_{OUT} = V_{CC}\left(\sqrt{\frac{R_{LOAD}T}{2L_1}}\right)D.$$

In the practical circuit of Figure 2, all of the elements of the basic flyback circuit of Figure 1 can be identified. However, there are a number of refinements that lead to better operation and stability. For example, two output diodes are configured so that dual-rail output is possible. Also, the positive rail feedback is sampled by the voltage divider comprising R4 and R5, with a level that is smoothed by capacitor C2. In normal 555 astable operation, the output waveform generation is possible since the timing capacitor (C1) charges from VCC through the sum of R1 and R2 and discharges through R2. With the resistor values used (that is, R2>>R1), the duty cycle is

close to 50%. The charging/discharging voltage levels are internally set to VCC/3 and 2VCC/3 (that is, 1.67V and 3.33V, respectively, if operated at 5V). Without feedback, the values in Figure 2 give an open-loop output voltage of about 20V. The feedback operates as follows: The transistor, Q1, does not conduct until the voltage at its base (VBE) is around 0.55V. This enables the output voltage to be calculated from

$$V_{OUT} = \left(1 + \frac{R_4}{R_5}\right)V_{BE}.$$

As the output voltage continues to increase under the action of flyback, Q1 is driven even harder, causing its collector voltage to fall. Since the collector is connected to the control input of the 555 timer that is nominally the upper limit above (2VCC/3), this causes the capacitor to charge and discharge at the same rate but through a narrower voltage range. This has the effect of reducing both the "on" and "off" times of
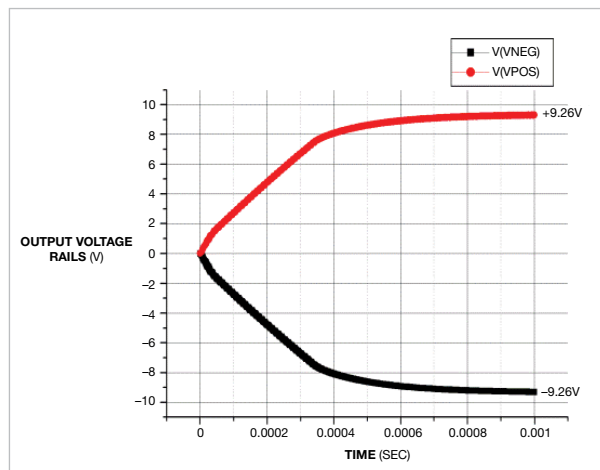
the output pulses that drive the MOSFET switch. The net variation in both the frequency and the duty cycle (D) causes VOUT to fall and eventually lower the feedback voltage, with the effect of reducing the "on" time of Q1.

One aspect of the circuit that needs careful setting up is the flyback transformer. Several home-made transformers were tried and worked reasonably well. The solution settled on was to reuse the core of an RFI suppression inductor commonly found at the mains input end of switched-mode power supplies in television sets. The windings of the transformer primary are multi-filar to reduce their series resistance. For example, using four strands of 0.3-mm insulated copper wire closely wound seven turns gave an inductance of 30 µH for the primary with a measured series resistance of 0.03Ω. A lower coil resistance reduces joule heating in the inductor as it is switched, leading to higher efficiency. A suitable commercially available ferrite core and bobbin set is available from RS-Electronics (RS stock number 647-9446, manufactured by Epcos).

A further refinement is the use of high-current, high-speed, and low-forward-voltage Schottky diodes for D1 and D2. An additional diode is used in reverse bias at the gate of the MOSFET to reduce RFI. Including a 100-mH choke on the 5V USB line also reduces switching noises further.

For the purposes of our design, the USB port was modelled as a 5V source with a series resistance of 10Ω for a worst-case current of 500 mA. A decoupling capacitor, C5, of 100 µF is used to prevent switching noises from being developed across the power rails. The measured output efficiency was around 72%, with a load of 50Ω, with the output voltage dropping to ±7.6V. The output has also been connected successfully to linear regulators such as the 78L05 for other voltages. A further design refinement is possible to make the output switchable under software control. We have not done it here, but some means of turning the 555 off or on using a separate active transistor would implement standby or active operation.

Figure 3 shows the turn-on transient response of the converter. Figure 4, available with the online version of this Design Idea at www.edn.com/4415896, shows that the circuit responds gracefully to a step load change 10 msec after turn-on. **EDN**

Figure 3 *At turn-on, the output stabilizes within 0.8 msec, with two loads of 200Ω each.*

H-bridge paves new ways for LED lighting

Subodh Johri and Prateek Johri, Central Electronics Engineering Research Institute (CSIR-CEERI), Pilani, Rajasthan, India

The H-bridge is a classic circuit used for driving dc motors in a user-defined manner, such as in forward/reverse direction or PWM-assisted controlled RPM with the help of four discrete/integrated switches or electromechanical relays. It is widely employed in robotics and power electronics. This Design Idea is a novel implementation of this technique for driving white-LED arrays directly from the ac mains in full-wave current-limited mode to realize an excellent flicker-free, energy-efficient solid-state lamp. The circuit controls and maintains the LED excitation current in both negative and positive half cycles of the excitation voltage to a constant level by way of electronic switches operating alternately during the positive and negative excursion of the excitation voltage. This approach facilitates current-controlled rectification of ac voltage into a dc voltage for energizing series-connected

LEDs with clean dc current with negligible ripple and substantially enhances the power factor.

As shown in Figure 1, transistors Q1, Q3, and Q5 and diode D4 as well as transistors Q2, Q4, and Q6 and diode D3 are configured as series-connected voltage-controlled current switches to form two arms of the H-bridge; diodes D1 and D2 form the other two arms of the bridge. The LED string is connected between the midpoints of the bridge designated as VLED+ and VLED GND, respectively. The ac is applied to the circuit through a current-limiting PTC resistor, R5; series-connected capacitors, C4 and C5 (configured as a nonpolar capacitor, CEFF); and inductor, L1. Likewise, the neutral side of the mains is connected to the circuit ground through an inductor, L2.

During the positive half cycle, the ac power bus becomes positive with respect to the ground, and transistor

Q1 gets appropriate base bias through resistor R1. Current flows through diode D4, transistor Q1, and resistor R3, as illustrated by arrow A1, and then through the LED string comprising 12 medium-power LEDs (LED1 to LED12) to the ground through diode D2, as shown by arrow A2. In a similar fashion, during the negative half cycle when the ac power bus becomes negative with respect to ground and transistor Q2 gets base bias through resistor R2, the current flows through diode D3, transistor Q2, and resistor R4, as illustrated by arrow A3, and then through the LED string to the ac power bus through diode D1, as shown by arrow A4. In this way, during a complete cycle the current flows through the string in the same direction and gets added up like you would get in a full-wave bridge rectifier. However, the magnitude of current ILED remains constant as regulated by the respective switches serving as voltage-controlled current sources.

As the base emitter junctions of transistors Q3 and Q4 are connected across current-sensing resistors R3 and R4, respectively, they turn on when the voltage drop across R3 and R4 increases beyond Q3 and Q4's base emitter voltages. At this point, Q1's and Q2's bases
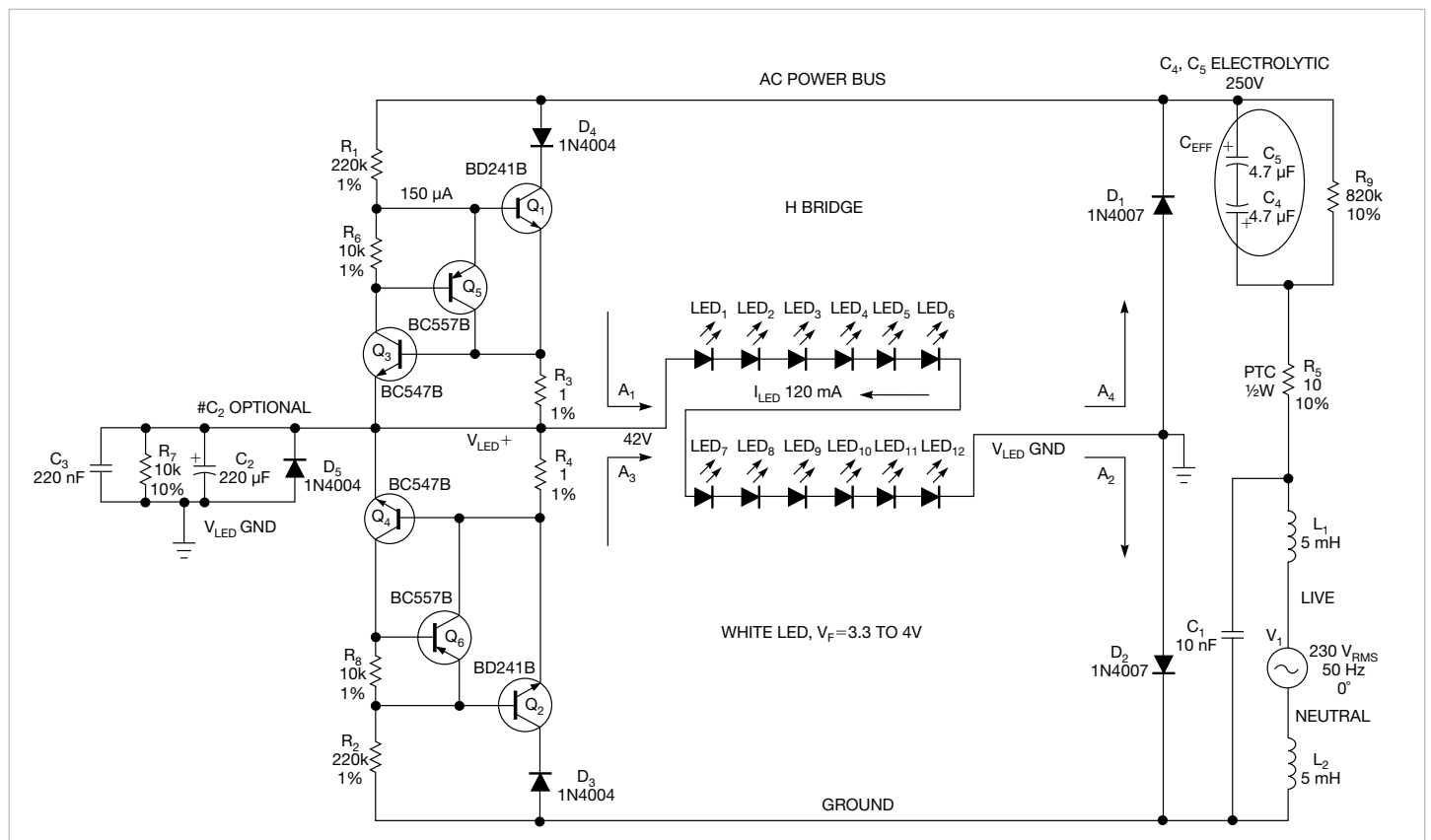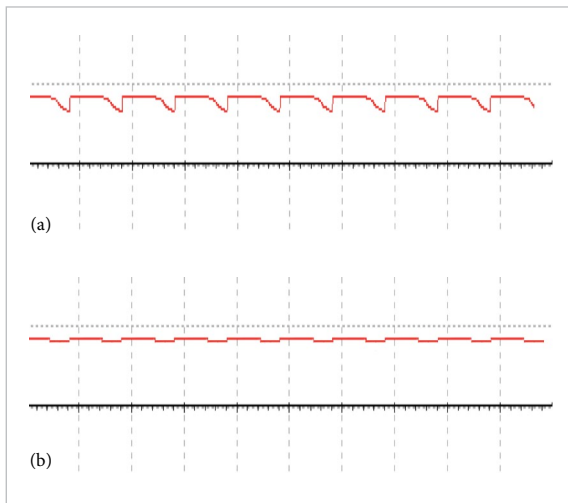

Figure 1 *Current-limiting transistors and diodes route alternate ac half cycles to the series LED string.*

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Figure 2 V_{LED}+ without capacitor C_2 has ripple (a); V_{LED}+ with capacitor C_2 has reduced ripple (b).

are pulled down, disrupting the flow of current through them during respective half cycles of the ac mains. In this way, the current flowing through the transistors is kept constant and never allowed to go beyond a threshold, set by appropriately choosing the R3 and R4 values. Q5 and Q6 limit the base current of Q1 and Q2 to a safe value (around 150 µA) to ensure that they are never overdriven. The substantial parts of the base cur-

rents of Q1 and Q2 are shunted to R3 and R4 by means of Q5 and Q6 when their respective base emitter voltages exceed the potential drop across R6 and R8 connected in series with R1 and R2, respectively.

The magnitude of ac current flowing into the bus is limited by the reactance of CEFF(1/2πfCEFF) at the mains frequency and can be altered by appropriately choosing C4 and C5, configured as a nonpolar capacitor. The circuit can also be driven by a resistive supply by replacing CEFF with a suitable high-power resistor of 50 to 200Ω. This may facilitate an excellent power factor, but at the expense of very high power losses in the current-limiting resistor. R3 and R4 can be chosen appropriately as per the required constant-current magnitude. D5 protects the LED string from high reverse voltage, and R5 limits the inrush of current at turn-on. Inductors L1 and L2 and capacitor C1 help in minimizing the EMI/RFI besides improving the power factor. A metal oxide varistor can also be inserted in parallel

with the ac mains to protect the circuit from transients.

In the circuit, 12 0.5W LEDs operate at 120-mA dc (135-mA RMS) with respect to current-sensing resistors R3 and R4, chosen as 1Ω. You can, however, increase the number of LEDs to 18 as long as the voltage being applied across the string is more than the sum of the forward voltage of the individual LEDs. (White LEDs' forward voltage varies from 3.3 to 4V.) The voltage appearing across the string is self-limiting (in this case, it is around 42V) and does not require any additional regulation, since series-connected LEDs behave like high-power zener diodes when operated in forward-biased mode. The circuit draws 11.5W power at 230V-ac RMS and exhibits a power factor of 0.93 without any perceptible flicker in the LEDs. You may optionally connect a 220-µF capacitor, C2, between VLED+ and VLED GND to further suppress ripple, as shown in Figure 2. Alternatively, the given string can be replaced by six parallel-connected strings of LEDs, each having 12 to 18 20-mA rated high-brightness LEDs. You must mount transistors Q1 and Q2 on heat sinks to avoid thermal runaway.**EDN**

Two ICs form F/V converter

Peter Winship, University of California, Berkeley

Using only six components, you can configure a circuit (Figure 1) whose output voltage is proportional to its input frequency. Moreover, only three of the components—capacitor C0, resistor R, and the OP-07 op amp—must exhibit low drift for stable operation over temperature. The circuit provides linear operation well into the megahertz region.

The average current (IAVG) from the 40106 Schmitt-trigger inverter's ground pin (pin 8) is linearly dependent on the frequency at which C0 is discharged into the op amp's summing junction. The op amp forces this current to flow through the 13.33-kΩ feedback resistor, producing a corresponding voltage drop. The output voltage is

$$V_0 = -V_{CC}RC_0f,$$

where f is the input frequency. Adjust the 10-kΩ potentiometer to calibrate the converter.

The 1- and 0.1-µF capacitors smooth the transients that result from the rapid switching. For the figure's values, the output ranges from 0 to −10V for inputs of 0 to 10 kHz. If you need higher-frequency operation, you must consider the effects of rapid switching on the CMOS inverter's supply current. Because a CMOS IC's power dissipation is proportional to frequency, you can simply add its supply current to the capacitor's discharge current in the calculations. You can make a frequency summer by exploiting the fact that there are six Schmitt triggers per package: Attach a capacitor to each inverter's output, apply a different frequency to each input, and obtain V0 proportional to the sum of the input frequencies:

$$V_0 = -V_{CC}R(C_1f_1 + C_2f_2 + \dots + C_6f_6).$$

Moreover, you can extend the technique by paralleling additional ICs.

With the figure's component values, the

F/V converter yields ±0.4% max nonlinearity for inputs of 0 to 10 kHz.**EDN**
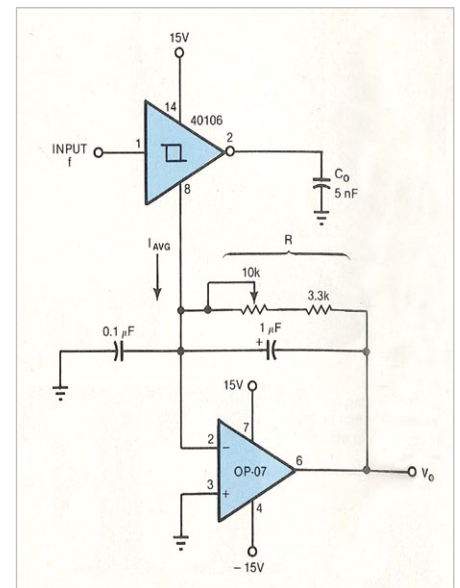
Figure 1 Using a capacitively loaded IC's supply-current/frequency dependence, this F/V converter yields 0 to −10V output with 0- to 10-kHz input frequencies. By paralleling more Schmitt triggers, you can use the circuit as a frequency summer.
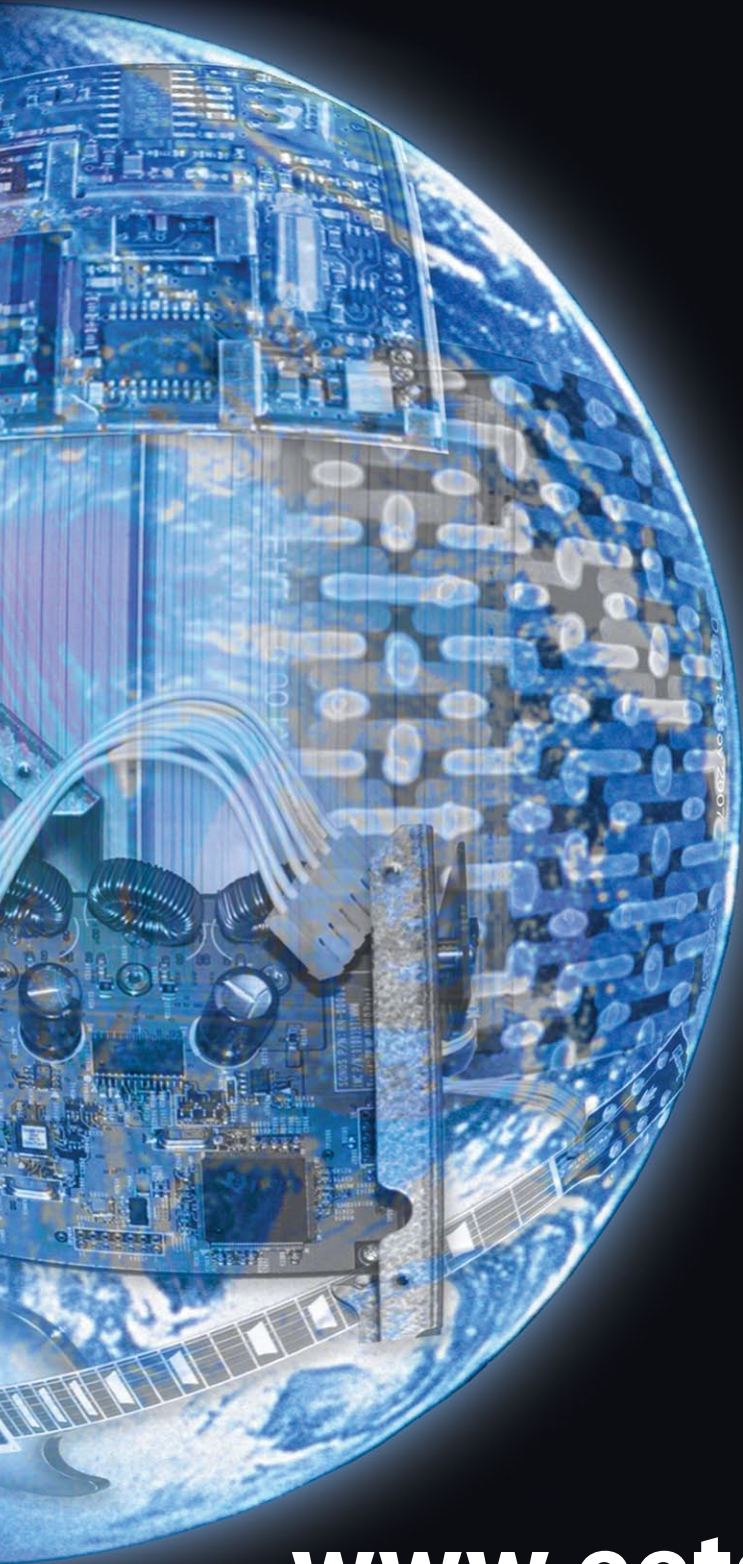
productroundup

12-bit PCIe digitiser for multi-GHz processing

Agilent Technologies' U5303A is a compact dual-channel PCIe digitiser with 12-bit resolution, sampling up to 3.2 Gsamples/sec, and on-board real-time processing. It delivers, Agilent says, unprecedented analogue fidelity, high effective number of bits and very low noise. The digitiser occupies a small footprint and offers DC-to-2 GHz bandwidth, 9.1 ENOB at 100 MHz, 58 dB signal-to-noise ratio and very high data-transfer rates from an eight-lane PCIe 2.0 interface. The U5303A gives users the ability to integrate advanced real-time signal processing within

its embedded Xilinx Virtex-6 field-programmable gate array. This is made possible by the Agilent FPGA development kit for high-speed digitisers. This software kit provides interfaces that leverage the full density and speed of the FPGA while ensuring the digitiser's outstanding level of performance at multi-gigasamples per second.

Agilent; high-speed-digitizer.tm.agilent.com

40-V, 1.5-A linear regulator

LT3081 is a rugged 1.5-A wide input voltage range linear regulator with an extended safe operating area (SOA), for high input-to-output voltage and high output current applications where older regulators limit the output. The LT3081 uses a current source reference for single resistor output voltage settings and output adjustability down to zero. Output current limit can be set externally with a single resistor. This regulator architecture, combined with low millivolt regulation, enables multiple ICs to be paralleled for heat spreading and higher output current. The current from the device's current monitor can be summed with the set current for line-drop compensation. The LT3081 achieves line and load regulation of under 2mV independent of output voltage and has an input voltage range
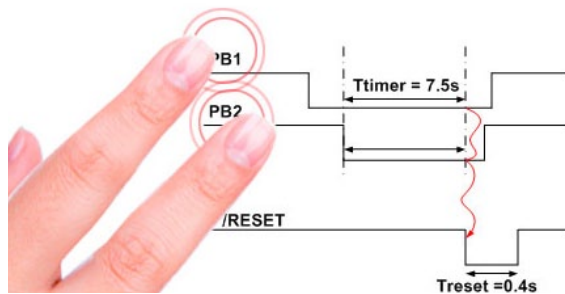
from 1.2V to 40V. The device fits applications requiring multiple rails. Output voltage is programmable with a single resistor from 0V to 38.5V with a 1.2V dropout. The on-chip trimmed 50 µA current reference is ±1% accurate. Current limit, accurate to ±10%, can be programmed with a single resistor. Monitor outputs provide a current output proportional to temperature (1 µA/°C) and output current (200 µA/A), allowing ground-based measurement. The LT3081's internal protection circuitry includes reverse input protection, reverse-current protection, internal current limiting and thermal shutdown. The LT3081 is offered in a variety of thermally enhanced surface-mount compatible packages; pricing starts at $2.60 (1000).

**Linear Technology; www.linear.com/product/LT3081**

Safety-critical software for ARM Cortex

Vector Software has announced support for the AdaCore GNAT Pro Compiler for ARM Cortex-based devices, enhancing Vector Software's offering for embedded Ada software development. The AdaCore GNAT Pro Safety-Critical application provides a complete Ada development environment, oriented towards systems that have safety-critical or stringent memory constraints requirements. Vector Software's VectorCAST embedded software testing platform is a family of products that automates testing activities across the software development lifecycle and supports C, C++, and Ada. VectorCAST includes a suite of Ada test tools that significantly reduces the time, effort, and cost associated with testing safety-critical software written in Ada. Support for ARM by AdaCore and VectorCAST allow organisations developing safety-critical applications for ARM in Ada, or a combination of Ada, C, and C++, to have a complete Ada development and automated testing environment.

Vector Software; www.vectorcast.com

Smallest SMD pulse transformer for LANs

With a size of 3.2 x 3.2 x 2.8 mm and occupying 30% less volume and smaller footprint than existing products, these TDK transformers claim more stable product quality thanks to an automated winding process. The inductance of the ALT3232M transformer is 150 µH, its insertion loss is in the frequency range from 100 kHz to 100 MHz at 2.5 dB, and its parasitic winding capacitance is only 25 pF at 100 kHz. By applying technology developed for production of SMD common mode filters, TDK was able to devise an automated winding process suitable for mass production. This reduces characteristics variations that tend to occur with manual winding, and thereby offers enhanced reliability and quality.
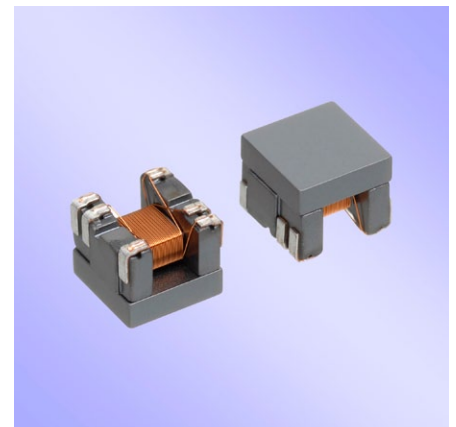
TDK, www.global.tdk.com

Low-noise timing chipset for basestations

IDT has announced a low-noise timing chipset for use in wireless base transceiver station (BTS) radio cards, enabling solutions to phase noise-related challenges in wireless systems. IDT 8V19N4xx comprises a flexible JESD204B-compliant radio frequency phase-locked loop (RF PLL) and clock synthesiser, designed to meet both the high frequency and low phase noise requirements for 2G, 3G and 4G LTE wireless infrastructure. Using IDT's FemtoClock NG technology, the low phase noise characteristics enable the system's ADCs and DACs to function with high precision and very low distortion levels. This results in improved signal integrity on transmission and enhanced signal sensitivity on reception, increasing data throughput via lower bit error rates (BER). Reduced noise in the RF signal path enables base-station developers to decrease cost and complexity by relaxing the system's filter requirements. The chipset generates synchronised and highly-configurable clock and SYSREF signals as required by JESD204B applications. This allows designers to use a standard, cost-effective timing chipset with a high degree of flexibility instead of multiple PLLs, synthesisers, and buffers.

IDT; www.idt.com/go/timing

Fully-certified ESD-robust FlexRay transceiver
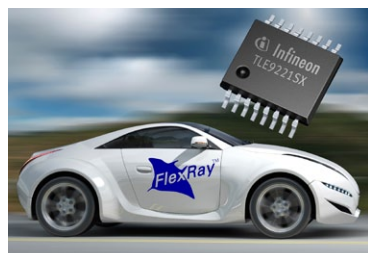
Infineon is expanding its portfolio of LIN and CAN automotive communications ICs with its first FlexRay transceiver. The TLE9221SX is fully compliant to the most current FlexRay Electrical Physical Layer Specification version 3.0.1. It enables very high data rates of up to 10 Mbit/sec for in-vehicle communication and features ESD rating of ±10 kV. The TLE9221SX transceiver was developed for use in suspension and chassis control applications as well as for power steering, engine and transmission control units; Infineon reports a trend towards extending the FlexRay bus from chassis control and body gateway applications to the powertrain domain, including engine and transmission control. The TLE9221SX has very low electromagnetic emissions (EME) and therefore supports large networks and complex bus topologies. It is also optimised for high immunity against electromagnetic interferences (EMI). The 16-pin TLE9221SX can easily be integrated into existing designs, because it can be placed on a 20-pin FlexRay transceiver footprint. Its bus pins are protected against short circuits to positive as well as negative battery voltage levels.

Infineon;
www.infineon.com/flexray-transceiver and
www.infineon.com/automotive-transceivers

Primary-side PSU controller with BJT driver

CamSemi (Cambridge Semiconductor) has announced advances in its bipolar transistor (BJT) drive scheme and the first of a new series of Primary Side Sensing (PSS) controllers. The C2172 PSS controller will enable lowest cost, most energy-efficient BJT-based solutions for mobile phone chargers and other universal input applications rated to 6.5 W. The new drive scheme will also help designers improve the ruggedness of their designs. CamSemi's BJT drive technology uses combined base and emitter switching to boost switching performance and deliver higher operating efficiencies, more Reverse Bias Safe Operating Area (RB-SOA) margin and the flexibility to accommodate a wide range of low cost BJTs. C2172 combines this drive scheme with the company's PSS technology to deliver no-load power consumptions well below 30 mW and good load-transient response but with significantly lower system cost and component counts. C2172 also incorporates many of the same design benefits as the company's existing PSS controller families including: accurate current and voltage regulation of ±5% without board-level trimming; quasi-resonant switching to reduce EMI and to enable compliance with efficiency standards with additional manufacturing margin; and full protection features.
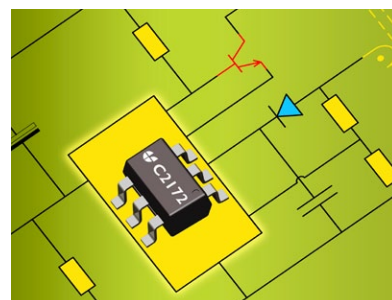
CamSemi; www.camsemi.com

Automotive thermal fuses break 55A

Vishay Intertechnology has introduced thermal fuses that offer high current capabilities up to 55A and operation at temperatures up to +160°C for 1,000 hours without unexpected breakdown. AEC-Q200-tested, devices in the new Vishay Beyschlag HCTF series provide a safety interrupt of electrical power in high-current automotive applications. In the case of excess heat in the range of the functioning temperature of +235°C (± 15 K), HCTF thermal fuses open automatically and disconnect the circuit. Typical applications for HCTF devices include automotive power electronics that can be connected to steady battery power. The thermal fuses offer significantly higher current capabilities than other devices on the market, which are limited to 25A at an ambient temperature of 23°C or 12A at an ambient temperature of 100°C. The HCTF devices' solid-state design, in combination with low cold resistance of ≤ 0.1 mΩ, guarantees extended reliability at high current loads and ambient temperatures.
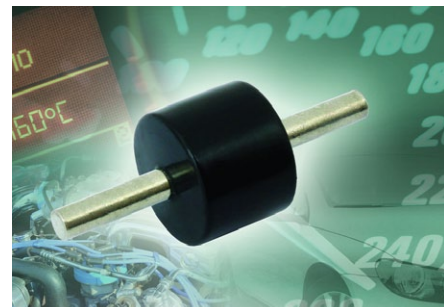
Vishay Beyschlag; www.vishay.com

productroundup

Raspberry Pi becomes a media centre

The XBMC bundle allows users to quickly turn their Raspberry Pi computers into a low-cost home media centre. The XBMC bundle will allow users to stream content from devices on their home network through their Raspberry Pi, turning the screen or their TV into a media centre. The Raspberry Pi will then stream content from any computer on the local network. Users can also access their Xbox Live ID to recommend content. The XBMC bundle includes an SD card pre-loaded with Raspbmc software, an open source Linux distribution created by Sam Nazarko that brings Xbox Media Center (XBMC) to the Raspberry Pi. A straightforward user guide featuring an online video tutorial is included. To control the Raspberry Pi in XBMC mode, the bundle includes an ultra Mini Keyboard and integrated Mouse Pad that wirelessly connects to the Raspberry Pi, while HDMI and Ethernet cables are provided to connect to a TV or monitor and the Internet.

Element14;
www.element14.com/raspberrypi

Translucent flex antenna

Pulse Electronics' mLUX Translucent Flex Antenna enables more innovative, creative, and impressive design effects for mobile devices. The mLUX is an invisible antenna concept. It allows light and colour to shine through the translucent device cover, offering multiple options for industrial design. When integrated into the display, the antenna enables increased use of metal on the back cover of the handset. Total thickness of the flex is 130-185 µm with a copper thickness of 12 µm. Non-pattern areas are filled with mesh to achieve a surface that is equally reflective throughout. The Cu mesh line-width is 12-20 µm with 300 µm pitch and the flex transmittance is typically around 80%. The antenna can be used with all mobile connected devices such as mobile phones, smart phones, and tablets and is compatible with any radiator RF concept. The concept is suitable for cellular and complementary applications.

Pulse Electronics;
www.pulseelectronics.com/mLUX

Cree XLamp MK-R LEDs

Mouser Electronics is now stocking the XLamp MK-R LEDs from Cree, which use the SC^3 Technology next-generation LED platform to deliver up to 200 lumens-per-watt, a level that the company identifies as an industry milestone. Output of up to 200 l/W (at 1W, 25ºC) enables lighting manufacturers to create the next generation of high-lumen indoor and outdoor LED lighting systems. MK-R LEDs are available in EasyWhite colour temperatures, providing the LED best colour consistency for designs that use only one LED. For systems that use multiple LEDs, MK-R enables manufacturers to use fewer LEDs while still maintaining light output and quality, which translates to lower system cost. SC^3 Technology uses Cree's silicon-carbide technology, features advancements in LED chip architecture and phosphor, and has a new package design to deliver the most advanced LED components.
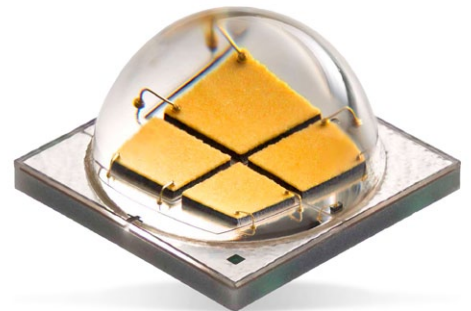
Mouser;
www.mouser.com/new/cree/cree-MKR/

Graphics memory & Cortex-A cores in Renesas MCUs

Renesas Electronics has disclosed the first products in its RZ family with large-capacity on-chip ram to enable DRAM-less design for high performance and low system cost; 10 MB of on-chip RAM is said to be the largest capacity available, allowing a WXGA display without external memory. There are five new products in the RZ/A1 Group of embedded micro-processor (MPU) solutions (with subcategories RZ/A1H, RZ/A1M, and RZ/A1L) for creating sophisticated human-machine interfaces (HMIs). Key features of the new products include 10 MB of on-chip RAM and capabilities needed to implement an HMI, such as camera input, hardware accelerated graphics output, OpenVG 1.1 and audio functions. Since there is no need for additional DRAM, developers of new products can implement a WXGA-resolution (1,280 x 768 pixels) graphics display without concerns about the long-term procurement of DRAM, while achieving improved system performance, reduced power consumption, and lower system cost overall. With on-chip RAM there are no bandwidth limitations imposed by the pin counts of the chips. Wide-band, low-latency memory access is possible, enabling overall system performance to be increased by as much as 30 to 50%. An ARM CPU allows developers to take advantage of the ARM tools ecosystem.
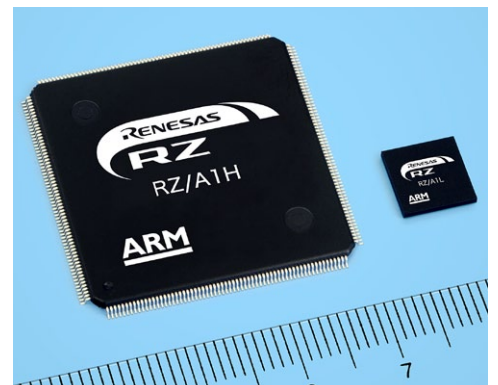
Renesas;
www.renesas.com/products/mpumcu/rz/rza/rza1/index.jsp#overview

Microsemi adds IGLOO2 mid-range FPGAs

Microsemi says that the non-volatile flash-based IGLOO2 FPGAs have the highest number of mainstream FPGA features including general purpose input/outputs (GPIOs), 5G SERDES interfaces, and PCI Express endpoints of any similar device, and feature the industry's only high-performance memory subsystem. When compared to other 5G SERDES-based FPGAs under 150k logic elements (LEs), IGLOO2's high level of integration provides the lowest total system cost while improving reliability, significantly reducing power and systematically protecting customers' valuable design IP. IGLOO2 mainstream FPGAs feature a LUT-based fabric, 5G transceivers, high-speed GPIO, block RAM and DSP blocks in a differentiated, cost- and power-optimised architecture. The architecture offers up to five times more logic density and three times more fabric performance than the previous generation IGLOO family. FPGA features are complemented by a built-in high-performance memory subsystem (HPMS) that embeds common user functions such as embedded SRAM memory blocks. These memories provide fast, predictable low latency to time-critical embedded applications such as video, embedded graphics functions and real-time Ethernet. Included in the HPMS is up to 512 kBytes of flash memory which allows users to store system data such as Ethernet MAC IDs, user keys, system configuration and system personalisation data. Pricing for IGLOO2 starts at less than $7 for high volume orders.

Microsemi, www.microsemi.com/igloo2-fpga

Glass-encapsulated varistors improved protection

The latest additions to AVX's TransGuard & Automotive TransGuard Series varistors extend bi-directional over-voltage protection and EMI/RFI attenuation benefits to high energy and harsh environment applications. These multilayer varistors provide bi-directional over-voltage protection and EMI/RFI attenuation in a single SMT package. The series also feature multi-strike capability, and sub 1-nsec response to ESD strikes. The TransGuard and Automotive TransGuard varistor series feature a high-energy, monolithic multilayer construction that provides circuit protection from voltage transients caused by ESD, lightning, inductive switching, automotive related transients, and other disruptions; with the addition of the high energy, glass-encapsulated options, an even broader range of applications can take advantage of the series' advanced, high-reliability circuit protection capabilities. For use in harsh environments – such as those with acid, salt, or chlorite flux – glass-encapsulated TransGuard and Automotive TransGuard Series varistors are available in three case sizes (1210, 1812, and 2220), four energy ratings (spanning 2-12J) and feature a peak current rating of up to 2000A. Both series also have Ni/Sn-plated terminations, are RoHS compliant, and are rated for use in temperatures spanning -55°C to +125°C.

AVX, www.avx.com

Fujitsu expands 32-bit ARM MCUs

FM4 32-bit microcontrollers based on the ARM Cortex-M4F processor core offer greater processing power plus floating point hardware support with half the per-frequency power consumption of the Fujitsu FM3 family. FM4 MCUs in the MB9B560R/460R/360R/160R series can operate from 3 V or 5 V power supplies, and offer a range of memory options that includes SRAM, NOR flash, NAND flash and SDRAM. The MCUs feature an ultra-wide bus for on-chip flash memory that enables read access with no CPU wait state, to accelerate processing and reduce power requirements. The Cortex-M4 core incorporates DSP and FPU functions for advanced computation. Algorithms for operating on-chip flash memory have been redesigned for greater speed and lower power consumption. The current required to run the real-time clock (RTC)

and power the device via the dedicated VBAT pin can be limited to approximately 1.5 µA, making these high-performance MCUs useful even for standby power-conscious applications. The FM4 family also includes new peripheral functionality and enhances existing functions. The analogue circuitry in previous versions has now been redesigned. New trimming functions deliver internal oscillator accuracy of ±2%. The D/A converter can achieve 12-bit resolution and the 12-bit A/D converter operates at twice the speed of previous versions. To support software design for functional safety and facilitate certification, FM4 microcontrollers feature a range of hardware functions such as ECC (Error Correction Code) Flash, CRC and MPU (Memory Protection Unit).

Fujitsu; http://emea.fujitsu.com/semiconductor

Blame the programmer!

The spring of 1974 saw me working in the technical assistance center (TAC) of a major Canadian telecommunications company. We provided second-level support for two different generations of computer-controlled telephone switching systems. The older system was implemented using discrete diode transistor logic (DTL); the newer system used SSI DTL.

These systems comprised fully duplicated Harvard processors that usually ran in parallel. A control console monitored the state of critical registers in the processors, and any difference in the contents of these register pairs would generate a hardware interrupt—bells ringing and volumes of paper spewing from the maintenance TTY—initiating diagnostic routines to isolate the problem.

Early one morning, we received a call from the foreman at a switching office an hour or so north of us, wondering about the parity failures that were being reported on his switch. We ran memory diagnostics on the processor logging the errors a number of times, never logging any errors; re-synced the processors; and waited for the next "audit." The parity failure flag had been set during the previous 15 min-utes, and again logged numerous errors.

The R/W memory on these systems was implemented using ferrite sheets—just like core but a lot denser. Each module contained 4K (16-bit) words and weighed about 80 lbs. Each SP1 switch would have four to 16 modules. When an error occurred in one of these modules, usually evidenced by the processors' dropping "sync," a printed report would identify the memory location in error.

We had a problem: The processors never dropped sync, and the memory exerciser did not report any problems. A few days of discussions with the manufacturer led nowhere. We couldn't even isolate the problem to a specific module.

Come the weekend, I headed up north and met with the switch foreman. Since this was an in-service telephone switch, we could not do anything that would disrupt processing. I had an idea.

A review of the processor schematics showed us that all of the parity error circuits were routed back to an SR flip-flop in the processor. The state of this flip-flop was read and reset once every 15 minutes by one of the audit routines. The maintenance counsel also had the capability to display register information for the "offline" processor. With a little trepidation, we mounted a couple of the CPU cards on extenders and ran a wire from the parity error flip-flop to the reset pin of the CPU stop flip-flop (a wired OR; this was DTL after all). We ran our memory exerciser and, with the CPU stopped, read the address of the failing memory location on the maintenance console, quickly isolating the problem to a single memory module.

It would have been nice to describe how we quickly swapped modules and went home for supper, but the truth is that we spent most of the day tweaking the various analog amplifiers in the memory module. When this failed to resolve the problem, we were told to swap the failing 80-lb module with one that wasn't failing to "prove" that we had isolated the problem.

It was late Sunday evening before we finally finished that task—the failing address moving as we expected. A replacement module arrived in time to be installed the following weekend.

In a quiet moment back at the TAC, I pulled out the source code. It looked good; it checked every word of the module under test, running various patterns through the memory. What had I missed?

The eureka moment came when I realized that the memory exerciser never checked the state of the parity error flip-flop. It was the memory parity bit line that had the problem, and since the data bus to the CPU did not include the parity bit, there was no way that the exerciser could determine the parity bit was in error!

Problem was solved, a snide note was sent to the manufacturer suggesting that it correct the shortcoming in the memory exerciser, and another feather was added to my cap—an important consideration when you are 23 years old and out to conquer the world! **EDN**